LTC4259

Quad IEEE 802.3af Power over Ethernet Controller with AC Disconnect

August 2003

FEATURES

- **Controls Four Independent –48V Powered Ethernet Ports**
- **Each Channel Includes:**
  - **IEEE 802®.3af Compliant PD Detection and Classification**
  - **Inrush Control**
  - **Short-Circuit Protection with Current Foldback**
  - **PD Disconnect Using AC or DC Sensing**
  - **Power Good Indication**
- Operates Autonomously or Controlled by I^{2}C™ Serial Interface
- 4-Bit Programmable Digital Address Allows Control of Up to 64 Channels
- Programmable $\overline{INT}$ Pin Eliminates Software Polling
- Current Limit Duty Cycle Protects External FETs

APPLICATIONS

- IP Phone Systems
- DTE Power Distribution
- IEEE 802.3af Compliant Systems

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DESCRIPTION

The LTC®4259 is a quad –48V Hot Swap™ controller designed for use in IEEE 802.3af compliant Power Sourcing Equipment (PSE). It consists of four independent channels, each with inrush control, short-circuit protection, complete powered device (PD) detection and classification capability, and programmable PD disconnect using AC or DC sensing. Used with power MOSFETs and passives, as in Figure 1, the LTC4259 can implement a complete IEEE 802.3af compliant PSE.

The LTC4259 can operate autonomously or be controlled by an I^{2}C serial interface. Up to 16 LTC4259s may coexist on the same data bus, allowing up to 64 powered Ethernet ports to be controlled with only two digital lines. Fault conditions are signaled with the $\overline{INT}$ pin to eliminate software polling.

External power switches, current sense resistors and diodes allow easy scaling of current and power dissipation levels and provide protection against voltage and current spikes and ESD events.

The LTC4259 is available in a 36-pin SSOP package.

Linear Technology also provides solutions for 802.3af powered device (PD) applications with the LTC4257.
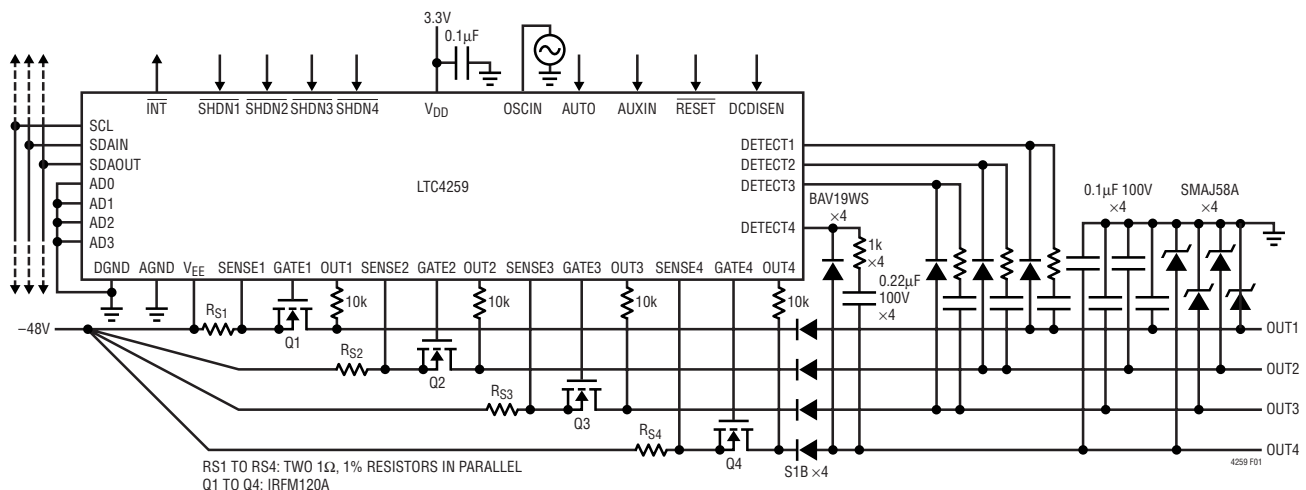
TYPICAL APPLICATION

Figure 1. Complete 4-Port Powered Ethernet Power Source

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ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages

V_{DD} to DGND .... −0.3V to 5V

V_{EE} to AGND .... 0.3V to −72V

DGND to AGND (Note 2) .... ±1V

Digital Pins

$\overline{SCL}$, SDAIN, $\overline{INT}$, AUTO, $\overline{RESET}$, AUXIN,

SHDN*n*, AD*n* .... DGND − 0.3V to DGND + 5V

Analog Pins

GATE*n* (Note 3) .... V_{EE} − 0.3V to V_{EE} + 12V

DETECT*n* (Note 4) .... ±80mA

SENSE*n* .... V_{EE} − 0.3V to V_{EE} + 1V

OUT*n* .... V_{EE} − 72V to V_{EE} + 72V

OSCIN .... DGND − 0.3V to DGND + 5V

Operating Temperature Range .... 0°C to 70°C

Storage Temperature Range .... −65°C to 125°C

Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

```
                 TOP VIEW
       ┌──────────────────────┐
RESET  │ 1                  36 │ OSCIN
AUXIN  │ 2                  35 │ AUTO
 INT   │ 3                  34 │ OUT1
 SCL   │ 4                  33 │ GATE1
SDAOUT │ 5                  32 │ SENSE1
SDAIN  │ 6                  31 │ OUT2
 AD3   │ 7                  30 │ GATE2
 AD2   │ 8                  29 │ SENSE2
 AD1   │ 9                  28 │ VEE
 AD0   │ 10                 27 │ OUT3
DETECT1│ 11                 26 │ GATE3
DETECT2│ 12                 25 │ SENSE3
DETECT3│ 13                 24 │ OUT4
DETECT4│ 14                 23 │ GATE4
 DGND  │ 15                 22 │ SENSE4
 VDD   │ 16                 21 │ AGND
SHDN1  │ 17                 20 │ SHDN4
SHDN2  │ 18                 19 │ SHDN3
       └──────────────────────┘
         GW PACKAGE
     36-LEAD PLASTIC SSOP

  $T_{JMAX}$ = 125°C, $\theta_{JA}$ = 80°C/W
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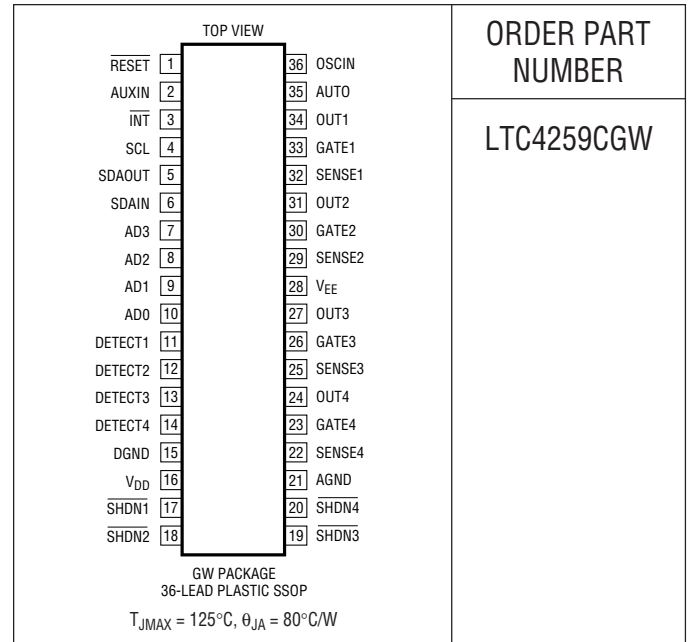
ORDER PART NUMBER
LTC4259CGW

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specificatiions which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 3.3V, V_{EE} = −48V unless otherwise noted (Note 5).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supplies							
V_{DD}	V_{DD} Supply Voltage		●	3	3.3	4	V
V_{EE}	V_{EE} Supply Voltage	To Maintain IEEE Compliant Output (Note 6)	●	−45.5	−48	−57	V
I_{DD}	V_{DD} Supply Current		●		2.5	10	mA
I_{EE}	V_{EE} Supply Current	Normal Operation During Classification	●		2	10 75	mA mA
ΔV_{GND}	DC Ground Difference	AGND − DGND	●	−0.1		0.1	V
V_{DDMIN}	V_{DD} UVLO Voltage				2.7		V
$V_{EEMINON}$	V_{EE} UVLO Voltage (Turning On)	V_{EE} − AGND			−31		V
$V_{EEMINOFF}$	V_{EE} UVLO Voltage (Turning Off)	V_{EE} − AGND			−28		V
Detection							
I_{DET}	Detection Current	First Point, $V_{DETECTn}$ = −3.5V Second Point, $V_{DETECTn}$ = −10V	● ●	145 235		190 300	μA μA
V_{DET}	Detection Voltage Compliance	Open Circuit, Measured at DETECT*n* Pin	●		−20	−23	V
R_{DETMIN}	Minimum Valid Signature Resistance		●	15.2	17	19	kΩ
R_{DETMAX}	Maximum Valid Signature Resistance		●	26.7	29	33	kΩ
Classification							
V_{CLASS}	Classification Voltage	0mA < I_{CLASS} < 50mA, Measured at DETECT*n* Pin	●	−16.5	−18.6	−20.5	V
I_{CLASS}	Classification Current Compliance	V_{PORT} = 0V	●	55		75	mA
I_{TCLASS}	Classification Threshold Current	Class 0-1 Class 1-2 Class 2-3 Class 3-4 Class 4-Overcurrent	● ● ● ● ●	5.5 13 21 31 45	6.5 14.5 23 33 48	7.5 16 25 35 51	mA mA mA mA mA

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ELECTRICAL CHARACTERISTICS

The ● denotes the specificatiions which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 3.3V, V_{EE} = −48V unless otherwise noted (Note 5).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Driver							
I_{GON}	GATE Pin Current	Gate On, V_{GATEn} = V_{EE}	●	−30	−50	−70	μA
I_{GOFF}	GATE Pin Current	Gate Off, V_{GATEn} = V_{EE} + 5V	●	30	50	80	μA
I_{GPD}	GATE Pin Short-Circuit Pull-Down	V_{GATEn} = V_{EE} + 5V			100		mA
ΔV_{GATE}	External Gate Voltage ($V_{GATEn} - V_{EE}$)	I_{GATE} = −1μA	●	10	13	15	V
Output Voltage Sense							
V_{PG}	Power Good Threshold Voltage	$V_{OUTn} - V_{EE}$	●	1	2	3	V
I_{VOUT}	Out Pin Bias Current	0V > V_{OUT} > −10V				−6	μA
		−10V > V_{OUT} > −30V				−18	μA
		V_{OUT} = −48V			−20		μA
Current Sense							
V_{CUT}	Overcurrent Detection Sense Voltage	$V_{SENSEn} - V_{EE}$, V_{OUT} = V_{EE}	●	175	187.5	200	mV
V_{LIM}	Current Limit Sense Voltage	$V_{SENSEn} - V_{EE}$, V_{OUT} = V_{EE}	●	200	212.5	225	mV
V_{MIN}	DC Disconnect Sense Voltage	$V_{SENSEn} - V_{EE}$	●	2.5	3.75	5	mV
V_{SC}	Short-Circuit Sense Voltage				275		mV
I_{SENSE}	SENSE Pin Bias Current	V_{SENSEn} = V_{EE}			−40		μA
AC Disconnect (Note 7)							
R_{OSCIN}	Input Impedance of OSCIN Pin	−0.3V < V_{SINEIN} < 3.3V, f_{OSC} < 200Hz	●	200	300		kΩ
A_{VACD}	Voltage Gain OSCIN to DETECT1, 2	Channel Powered, PD Not Present	●	−2.7	−3	−3.3	V/V
	Voltage Gain OSCIN to DETECT3, 4	Channel Powered, PD Not Present	●	2.7	3	3.3	V/V
I_{ACDMAX}	AC Disconnect DETECTn Output Current	Channel Powered, $V_{DETECTn}$ =	●			±600	μA
I_{ACDMIN}	Remain Connected DETECTn Current	Channel Powered, $V_{DETECTn}$ = 3.4V	●	150	200	250	μA
Digital Interface							
V_{OLD}	Digital Output Low Voltage	SDAOUT, INT, I_{PIN} = 10mA	●			0.4	V
V_{ILD}	Digital Input Low Voltage	SCL, SDAIN	●			0.8	V
V_{IHD}	Digital Input High Voltage	SCL, SDAIN	●	2.4			V
R_{PU}	Pull-Up Resistor to V_{DD}	AD0 to AD3, $\overline{RESET}$, $\overline{SHDN}n$			50		kΩ
R_{PD}	Pull-Down Resistor to DGND	AUXIN, AUTO			50		kΩ
AC Characteristics							
t_{DETDLY}	Detection Delay	From Detect Command or Application of PD to Port to Detect Complete (Figure 2)	●	170		590	ms
t_{CLSDLY}	Classification Delay	From Successful Detect in Auto or Semiauto Mode to Class Complete (Figure 2)	●	10.1		52	ms
		From Classify Command in Manual Mode to Class Complete	●	10.1		420	ms
t_{CLASS}	Classification Duration	(Figure 2)	●	10.1		13	ms
t_{PON}	Power On Delay, Auto Mode	From Valid Detect to Port On in Auto Mode (Figure 2)	●			90	ms
		From Port On Command to GATE Pin Current = I_{GON}	●			1	ms
t_{START}	Maximum Current Limit Duration During Port Start-Up	t_{START1} = 0, t_{START0} = 0 (Figure 3)	●	50	60	70	ms
		t_{START1} = 0, t_{START0} = 1	●	25	30	35	ms
		t_{START1} = 1, t_{START0} = 0	●	100	120	140	ms
		t_{START1} = 1, t_{START0} = 1	●	200	240	280	ms
t_{ICUT}	Maximum Current Limit Duration After Port Start-Up	t_{ICUT1} = 0, t_{ICUT0} = 0 (Figure 3)	●	50	60	70	ms
		t_{ICUT1} = 0, t_{ICUT0} = 1	●	25	30	35	ms
		t_{ICUT1} = 1, t_{ICUT0} = 0	●	100	120	140	ms
		t_{ICUT1} = 1, t_{ICUT0} = 1	●	200	240	280	ms

ELECTRICAL CHARACTERISTICS

The ● denotes the specificatiions which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 3.3V, V_{EE} = −48V unless otherwise noted (Note 5).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC_{CLMAX}	Maximum Current Limit Duty Cycle		●	5.8	6.3	6.7	%
t_{DIS}	Disconnect Delay	t_{DIS1} = 0, t_{DIS0} = 0 (Figures 4, 5)	●	300	360	400	ms
		t_{DIS1} = 0, t_{DIS0} = 1	●	75	90	100	ms
		t_{DIS1} = 1, t_{DIS0} = 0	●	150	180	200	ms
		t_{DIS1} = 1, t_{DIS0} = 1	●	600	720	800	ms
t_{VMIN}	DC Disconnect Minimum Pulse Width Sensitivity	$V_{SENSEn} - V_{EE}$ > 5mV, V_{OUTn} = −48V (Figure 4)	●		0.02	1	ms
I²C Timing							
f_{SCLK}	Clock Frequency	(Note 8)	●			400	kHz
t_1	Bus Free Time	Figure 6 (Notes 8, 9)	●	1.3			μs
t_2	Start Hold Time	Figure 6 (Notes 8, 9)	●	600			ns
t_3	SCL Low Time	Figure 6 (Notes 8, 9)	●	1.3			μs
t_4	SCL High Time	Figure 6 (Notes 8, 9)	●	600			ns
t_5	Data Hold Time	Figure 6 (Notes 8, 9)	●	150			ns
t_6	Data Set-Up Time	Figure 6 (Notes 8, 9)	●	200			ns
t_7	Start Set-Up Time	Figure 6 (Notes 8, 9)	●	600			ns
t_8	Stop Set-Up Time	Figure 6 (Notes 8, 9)	●	600			ns
t_r	SCL, SDAIN Rise Time	Figure 6 (Notes 8, 9)	●	20		300	ns
t_f	SCL, SDAIN Fall Time	Figure 6 (Notes 8, 9)	●	20		150	ns
t_{FLTINT}	Fault Present to $\overline{INT}$ Pin Low	(Notes 8, 9, 10)	●	20		150	ns
$t_{STOPINT}$	Stop Condition to $\overline{INT}$ Pin Low	(Notes 8, 9, 10)	●	60		200	ns
t_{ARAINT}	ARA to $\overline{INT}$ Pin High Time	(Notes 8, 9)	●	20		300	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: DGND to AGND voltages beyond ±100mV will prevent proper operation of the classification function.

Note 3: An internal clamp limits the GATE pins to a minimum of 12V above V_{EE}. Driving this pin beyond the clamp may damage the part.

Note 4: When a port powers on or off, the transient voltage on the port couples through C_{DET} (Figure 15). The LTC4259 contains internal protection circuitry to withstand transient currents of up to 80mA for 5ms. As long as the absolute value of the current remains below 80mA, the LTC4259 will keep the voltage at the DETECTn pin within the absolute maximum voltage range. A properly sized R_{DET} will limit the current to less than 60mA.

Note 5: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground (AGND and DGND) unless otherwise specified.

Note 6: Voltage at the Ethernet connector must be at least −44V for IEEE 802.3af compliance. The minimum V_{EE} supply voltage must take account for the drop across the diode D_{AC} in Figure 15.

Note 7: Unless otherwise specified, AC disconnect specifications require the following conditions: the DETECTn pin is connected to the port as shown in Figure 1, a valid sine wave is applied to OSCIN, the OSCFAIL bit is cleared and AC disconnect is enabled.

Note 8: Guaranteed by design, not subject to test.

Note 9: Values measured at V_{ILD} and V_{IHD}.

Note 10: If fault occurs during an I²C transaction, $\overline{INT}$ pin will not be pulled down until a stop condition is present on the I²C bus.
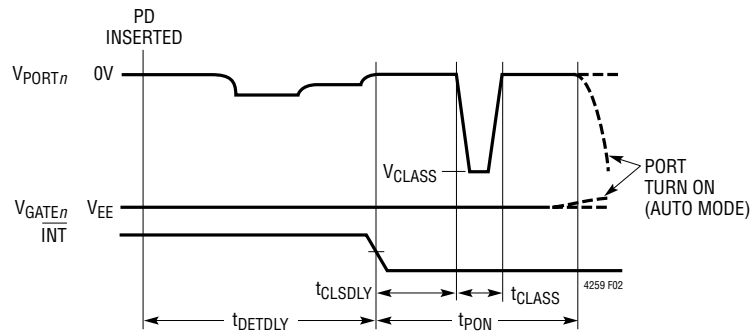
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TEST TIMING

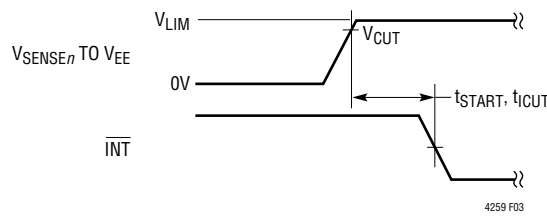**Figure 2. Detect, Class and Turn-On Timing in Auto or Semiauto Modes**
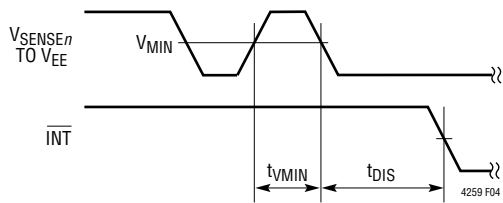

Figure 3. Current Limit Timing

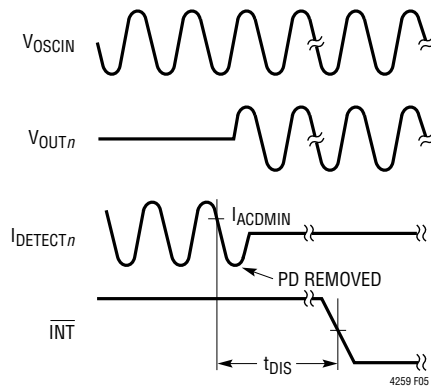**Figure 4. DC Disconnect Timing**

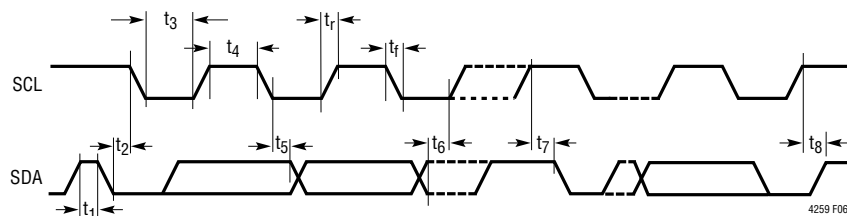**Figure 5. AC Disconnect Timing**

Figure 6. I²C Interface Timing
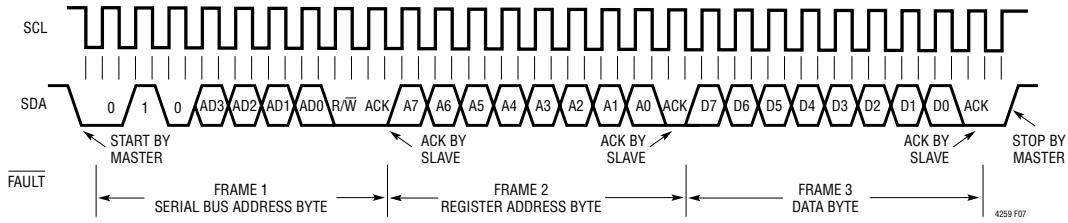
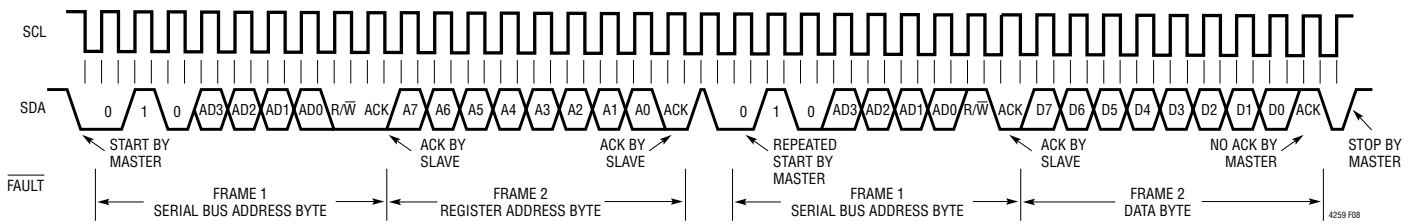# TIMING DIAGRAMS
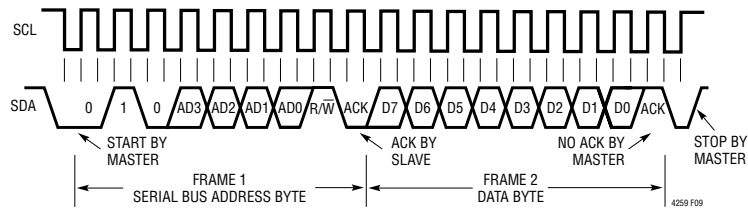

Figure 7. Writing to a Register

Figure 8. Reading from a Register
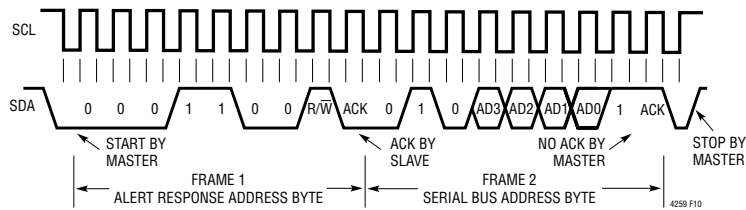

Figure 9. Reading the Interrupt Register (Short Form)

Figure 10. Reading from Alert Response Address

PIN FUNCTIONS

$\overline{\text{RESET}}$ **(Pin 1):** Chip Reset, Active Low. When the $\overline{\text{RESET}}$ pin is low, the LTC4259 is held inactive with all channels off and all internal registers reset to their power-up states. When $\overline{\text{RESET}}$ is pulled high, the LTC4259 begins normal operation. $\overline{\text{RESET}}$ can be connected to an external capacitor or RC network to provide a power turn-on delay. An internal 50k resistor pulls $\overline{\text{RESET}}$ high if not externally pulled down. Internal filtering of the $\overline{\text{RESET}}$ pin prevents glitches less than 1µs from resetting the LTC4259.

AUXIN (Pin 2): Auxiliary Input. The real time state of the AUXIN pin can be read at bit 1 in the Pin Status register (11h). An internal 50k resistor pulls AUXIN low if it is left floating. The AUXIN pin provides a simple way for the host controller to read the state of a switch or other human interface device.

$\overline{\text{INT}}$ **(Pin 3):** Interrupt Output, Open Drain. $\overline{\text{INT}}$ will pull low when any one of several events occur in the LTC4259. It will return to a high impedance state when bits 6 or 7 are set in the Reset PB register (1Ah). The $\overline{\text{INT}}$ signal can be used to generate an interrupt to the host processor, eliminating the need for continuous software polling. Individual $\overline{\text{INT}}$ events can be disabled using the Int Mask register (01h). See Register Functions and Applications Information for more information. The $\overline{\text{INT}}$ pin is only updated between I^{2}C transactions.

SCL (Pin 4): Serial Clock Input. High impedance clock input for the I^{2}C serial interface bus. The SCL pin should be connected directly to the I^{2}C SCL bus line.

SDAOUT (Pin 5): Serial Data Output, Open Drain Data Output for the I^{2}C Serial Interface Bus. The LTC4259 uses two pins to implement the bidirectional SDA function to simplify optoisolation of the I^{2}C bus. To implement a standard bidirectional SDA pin, tie SDAOUT and SDAIN together. See Applications Information for more information.

SDAIN (Pin 6): Serial Data Input. High impedance data input for the I^{2}C serial interface bus. The LTC4259 uses two pins to implement the bidirectional SDA function to simplify optoisolation of the I^{2}C bus. To implement a standard bidirectional SDA pin, tie SDAOUT and SDAIN together. See Applications Information for more information.

AD3 (Pin 7): Address Bit 3. Tie the address pins high or low to set the I^{2}C serial address to which LTC4259 responds. This address will be $(010A_3A_2A_1A_0)_b$. An internal 50k resistor pulls AD3 high if it is left floating.

AD2 (Pin 8): Address Bit 2. See AD3.

AD1 (Pin 9): Address Bit 1. See AD3.

AD0 (Pin 10): Address Bit 0. See AD3.

DETECT1 (Pin 11): Detection Sense, Channel 1. The LTC4259 powered device (PD) detection and AC disconnect hardware monitors port 1 with this pin. Connect DETECT1 to the port 1 output via a 100V 75mA signal diode in parallel with a 0.2µF 100V X7R capacitor in series with a 1k resistor (see Figure 1). The resistor and capacitor may be eliminated if AC disconnect is not used.

DETECT2 (Pin 12): Detection Sense, Channel 2. See DETECT1.

DETECT3 (Pin 13): Detection Sense, Channel 3. See DETECT1.

DETECT4 (Pin 14): Detection Sense, Channel 4. See DETECT1.

DGND (Pin 15): Digital Ground. DGND should be connected to the return from the 3.3V supply. DGND and AGND should typically be tied together. However, DGND can be separated from AGND by as musch as ±100mV and remain IEEE compliant.

V$_{DD}$ (Pin 16): Logic Power Supply. Connect to a 3.3V power supply relative to DGND. V$_{DD}$ must be bypassed to DGND near the LTC4259 with at least a 0.1µF capacitor.

$\overline{\text{SHDN1}}$ **(Pin 17):** Shutdown Channel 1, Active Low. When pulled low, $\overline{\text{SHDN1}}$ shuts down channel 1, regardless of the state of the internal registers. Pulling $\overline{\text{SHDN1}}$ low is equivalent to setting the Reset Port 1 bit in the Reset Pushbutton register (1Ah). An internal 50k resistor pulls $\overline{\text{SHDN1}}$ high if it is left floating and an internal filter with a time constant greater than 1µs prevents glitches from shutting down the port.

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PIN FUNCTIONS

$\overline{\text{SHDN2}}$ **(Pin 18):** Shutdown Channel 2, Active Low. See SHDN1.

$\overline{\text{SHDN3}}$ **(Pin 19):** Shutdown Channel 3, Active Low. See SHDN1.

$\overline{\text{SHDN4}}$ **(Pin 20):** Shutdown Channel 4, Active Low. See SHDN1.

AGND (Pin 21): Analog Ground. AGND should be connected to the return from the –48V supply. AGND and DGND should typically be tied together. However, if they are not, AGND can be separated from DGND by no more than ±100mV.

SENSE4 (Pin 22): Channel 4 Current Sense Input. SENSE4 monitors the external MOSFET current via a 0.5Ω sense resistor between SENSE4 and V_{EE}. Whenever the voltage across the sense resistor exceeds the overcurrent detection threshold V_{CUT}, the current limit fault timer counts up. If the voltage across the sense resistor reaches the current limit threshold V_{LIM} (typically 25mV/50mA higher), the GATE4 pin voltage is lowered to maintain constant current in the external MOSFET. See Applications Information for further details. If the channel is unused, the SENSE4 pin must be tied to V_{EE}.

GATE4 (Pin 23): Channel 4 Gate Drive. GATE4 should be connected to the gate of the external channel 4 MOSFET. When the MOSFET is turned on, a 50μA pull-up current source is connected to the pin. The gate voltage is clamped to 13V (typ) above V_{EE}. During a current limit condition, the voltage at GATE4 will be reduced to maintain constant current through the external MOSFET. If the fault timer expires, GATE4 is pulled down with 50μA, turning the MOSFET off and recording a t_{ICUT} or t_{START} event. If the channel is unused, float the GATE4 pin or tie it to V_{EE}.

OUT4 (Pin 24): Channel 4 Output Voltage Monitor. OUT4 should be connected to the output port through a 10k series resistor. A current limit foldback circuit limits the power dissipation in the external MOSFET by reducing the current limit threshold when the output voltage is within 18V of AGND. The port 4 Power Good bit is set when the voltage from OUT4 to V_{EE} drops below 2V (typ). A 2.5MΩ resistor is connected internally from OUT4 to AGND. If the

channel is unused, the OUT4 pin can be tied to AGND or allowed to float.

SENSE3 (Pin 25): Channel 3 Current Sense Input. See SENSE4.

GATE3 (Pin 26): Channel 3 Gate Drive. See GATE4.

OUT3 (Pin 27): Channel 3 Output Voltage Monitor. See OUT4.

V_{EE} (Pin 28): –48V Supply Input. Connect to a –45.5V to –57V supply, relative to AGND.

SENSE2 (Pin 29): Channel 2 Current Sense Input. See SENSE4.

GATE2 (Pin 30): Channel 2 Gate Drive. See GATE4.

OUT2 (Pin 31): Channel 2 Output Voltage Monitor. See OUT4.

SENSE1 (Pin 32): Channel 1 Current Sense Input. See SENSE4.

GATE1 (Pin 33): Channel 1 Gate Drive. See GATE 4.

OUT1 (Pin 34): Channel 1 Output Voltage Monitor. See OUT4.

AUTO (Pin 35): Auto Mode Input. Auto mode is intended to allow the LTC4259 to detect and power up a PD even if there is no host controller present on the I^{2}C bus. When this pin is high, all Mode bits in the Operating Mode register will be set at power-up or after a system reset. When this pin is low, all Mode bits will be cleared at power-up or after a system reset. The states of the Mode bits can be subsequently changed via the I^{2}C interface if desired. The real-time state of the AUTO pin can be read at bit 0 in the Pin Status register (11h). An internal 50k resistor pulls AUTO low if it is left floating.

OSCIN (Pin 36): Oscillator Input. Connect to an oscillating signal source, preferably a sine wave, of approximately 100Hz with 2V peak-to-peak amplitude, negative peaks above –0.3V and positive peaks below 2.5V. When a channel is powered and AC disconnect is enabled, this signal is used to detect the AC impedance of the PD.

TABLE 1. REGISTER MAP

ADDRESS	REGISTER NAME	R/W	PORT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET STATE Auto Pin Low	RESET STATE Auto Pin High
Interrupts													
00h	Interrupt	RO	Global	Supply Event	t_{START} Fault	t_{ICUT} Fault	Class Complete	Detect Complete	Disconnect	Pwr Good Event	Pwr Enable Event	1000,0000	1000,0000
01h	Int Mask	R/W	Global	Mask 7	Mask 6	Mask 5	Mask 4	Mask 3	Mask 2	Mask 1	Mask 0	1000,0000	1110,0100
Events													
02h	Power Event	RO	4321	Pwr Good Change 4	Pwr Good Change 3	Pwr Good Change 2	Pwr Good Change 1	Pwr Enable Change 4	Pwr Enable Change 3	Pwr Enable Change 2	Pwr Enable Change 1	0000,0000	0000,0000
03h	Power Event CoR	CoR	4321										
04h	Detect Event	RO	4321	Class Complete 4	Class Complete 3	Class Complete 2	Class Complete 1	Detect Complete 4	Detect Complete 3	Detect Complete 2	Detect Complete 1	0000,0000	0000,0000
05h	Detect Event CoR	CoR	4321										
06h	Fault Event	RO	4321	Disconnect 4	Disconnect 3	Disconnect 2	Disconnect 1	t_{ICUT} Fault 4	t_{ICUT} Fault 3	t_{ICUT} Fault 2	t_{ICUT} Fault 1	0000,0000	0000,0000
07h	Fault Event CoR	CoR	4321										
08h	t_{START} Event	RO	4321	Reserved	Reserved	Reserved	Reserved	t_{START} Fault 4	t_{START} Fault 3	t_{START} Fault 2	t_{START} Fault 1	0000,0000	0000,0000
09h	t_{START} Event CoR	CoR	4321										
0Ah	Supply Event	RO	4321	Over Temp	Reserved	V_{DD} UVLO	V_{EE} UVLO	Reserved	Reserved	OSC Fail	Reserved	0011,0010**	0011,0010**
0Bh	Supply Event CoR	CoR	4321										
Status													
0Ch	Port 1 Status	RO	1	Reserved	Class Status 2	Class Status 1	Class Status 0	Reserved	Detect Status 2	Detect Status 1	Detect Status 0	0000,0000	0000,0000
0Dh	Port 2 Status	RO	2	Reserved	Class Status 2	Class Status 1	Class Status 0	Reserved	Detect Status 2	Detect Status 1	Detect Status 0	0000,0000	0000,0000
0Eh	Port 3 Status	RO	3	Reserved	Class Status 2	Class Status 1	Class Status 0	Reserved	Detect Status 2	Detect Status 1	Detect Status 0	0000,0000	0000,0000
0Fh	Port 4 Status	RO	4	Reserved	Class Status 2	Class Status 1	Class Status 0	Reserved	Detect Status 2	Detect Status 1	Detect Status 0	0000,0000	0000,0000
10h	Power Status	RO	4321	Power Good 4	Power Good 3	Power Good 2	Power Good 1	Power Enable 4	Power Enable 3	Power Enable 2	Power Enable 1	0000,0000	0000,0000
11h	Pin Status	RO	Global	Reserved	Reserved	AD3 Pin Status	AD2 Pin Status	AD1 Pin Status	AD0 Pin Status	AUXIN Pin Status	Auto Pin Status	00A3A2A1A0a0*	00A3A2A1A0a1*
Configuration													
12h	Operating Mode	R/W	4321	Port 4 Mode 1	Port 4 Mode 0	Port 3 Mode 1	Port 3 Mode 0	Port 2 Mode 1	Port 2 Mode 0	Port 1 Mode 1	Port 1 Mode 0	1111,1111	1111,1111
13h	Disconnect Enable	R/W	4321	AC Discon En 4	AC Discon En 3	AC Discon En 2	AC Discon En 1	DC Discon En 4	DC Discon En 3	DC Discon En 2	DC Discon En 1	1111,0000	1111,0000
14h	Detect/Class Enable	R/W	4321	Class Enable 4	Class Enable 3	Class Enable 2	Class Enable 1	Detect Enable 4	Detect Enable 3	Detect Enable 2	Detect Enable 1	1111,1111	1111,1111
15h	Reserved	R/W		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0000,0000	0000,0000
16h	Timing Config	R/W	Global	Reserved	Reserved	t_{START}1	t_{START}0	t_{ICUT}1	t_{ICUT}0	t_{DIS}1	t_{DIS}0	0000,0000	0000,0000
17h	Misc Config	R/W	Global	Interrupt Pin Enable	Reserved	OSC Fail Mask	Reserved	Reserved	Reserved	Reserved	Reserved	1010,0000	1010,0000
Pushbuttons													
18h	Det/Class Restart PB	WO	4321	Restart Class 4	Restart Class 3	Restart Class 2	Restart Class 1	Restart Detect 4	Restart Detect 3	Restart Detect 2	Restart Detect 1	0000,0000	0000,0000
19h	Power Enable PB	WO	4321	Power Off 4	Power Off 3	Power Off 2	Power Off 1	Power On 4	Power On 3	Power On 2	Power On 1	0000,0000	0000,0000
1Ah	Reset PB	WO	Global	Clear All Interrupts	Clear Interrupt Pin	Reserved	Reset All	Reset Port 4	Reset Port 3	Reset Port 2	Reset Port 1	0000,0000	0000,0000

Key:
RO = Read Only
R/W = Read/Write
CoR = Clear on Read
WO = Write Only

* a: state of AUXIN pin
** the start-up state of the V_{EE} UVLO bit depends on the order the V_{DD} and V_{EE} supplies are brought up

Encoding

CLASS STATUS	
000	Class Status Unknown
001	Class 1
010	Class 2
011	Class 3
100	Class 4
101	Undefined—Read as Class 0
110	Class 0
111	Overcurrent

DETECT STATUS	
000	Detect Status Unknown
001	Short Circuit (<1V)
010	Reserved
011	RLOW (<15k)
100	Detect Good (15k < R < 33k)
101	RHIGH (>33k)
110	Open Circuit
111	Reserved

MODE BIT ENCODING		
00	Shutdown	Power Off, Detection and Class Off
01	Manual	Will Not Advance Between States
10	Semiauto	Detect and Class But Wait to Turn On Power
11	Auto	Detect, Class and Power Automatically

REGISTER FUNCTIONS

Interrupt Registers

Interrupt (Address 00h): Interrupt Register, Read Only. A transition to logical 1 of any bit in this register will assert the INT pin (Pin 3) if the corresponding bit in the Int Mask register is set. Each bit is the logical OR of the corresponding bits in the Event registers. The Interrupt register is Read Only and its bits cannot be cleared directly. To clear a bit in the Interrupt register, clear the corresponding bits in the appropriate Status or Event registers.

Int Mask (Address 01h): Interrupt Mask, Read/Write. A logic 1 in any bit of the Int Mask register allows the corresponding Interrupt register bit to assert the INT pin if it is set. A logic 0 in any bit of the Int Mask register prevents the corresponding Interrupt bit from affecting the INT pin. The actual Interrupt register bits are unaffected by the state of the Int Mask register.

Event Registers

Power Event (Address 02h): Power Event Register, Read Only. The lower four bits in this register indicate that the corresponding port Power Enable status bit has changed; the logical OR of these four bits appears in the Interrupt register as the Pwr Enable Event bit. The upper four bits indicate that the corresponding port Power Good status bit has changed; the logical OR of these four bits appears in the Interrupt register as the Pwr Good Event bit. The Power Event bits latch high and will remain high until cleared by reading from address 03h.

Power Event CoR (Address 03h): Power Event Register, Clear on Read. Read this address to clear the Power Event register. Address 03h returns the same data as address 02h and reading address 03h clears all bits at both addresses.

Detect Event (Address 04h): Detect Event Register, Read Only. The lower four bits in this register indicate that at least one detection cycle for the corresponding port has completed; the logical OR of these four bits appears in the Interrupt register as the Detect Complete bit. The upper four bits indicate that at least one classification cycle for the corresponding port has completed; the logical OR of these four bits appears in the Interrupt register as the Class Complete bit. In Manual mode, this register indicates that the requested detection/classification cycle has completed and the LTC4259 is awaiting further instructions. In Semiauto or Auto modes, these bits indicate that the Detect Status and Class Status bits in the Port Status registers are valid. The Detect Event bits latch high and will remain high until cleared by reading from address 05h.

Detect Event CoR (Address 05h): Detect Event Register, Clear on Read. Read this address to clear the Detect Event register. Address 05h returns the same data as address 04h, and reading address 05h clears all bits at both addresses.

Fault Event (Address 06h): Fault Event Register, Read Only. The lower four bits in this register indicate that a t_{ICUT} fault has occurred at the corresponding port; the logical OR of these four bits appears in the Interrupt register as the t_{ICUT} Fault bit. The upper four bits indicate that a Disconnect event has occurred at the corresponding port; the logical OR of these four bits appears in the Interrupt register as the Disconnect bit. The Fault Event bits latch high and will remain high until cleared by reading from address 07h.

Fault Event CoR (Address 07h): Fault Event Register, Clear on Read. Read this address to clear the Fault Event register. Address 07h returns the same data as address 06h and reading address 07h clears all bits at both addresses.

t_{START} Event (Address 08h): t_{START} Event Register, Read Only. The lower four bits in this register indicate that a t_{START} fault has occurred at the corresponding port; the logical OR of these four bits appears in the Interrupt register as the t_{START} Fault bit. The t_{START} Event bits latch high and will remain high until cleared by reading from address 09h. The upper four bits in this register are reserved and will always read as 0.

t_{START} Event CoR (Address 09h): t_{START} Event Register, Clear on Read. Read this address to clear the Fault Event register. Address 09h returns the same data as address 08h and reading address 09h clears all bits at both addresses.

Supply Event (Address 0Ah): Supply Event Register, Read Only. Bit 1, Osc Fail, sets when the signal at Pin 36, OSCIN, is absent or does not have the required amplitude and AC disconnect cannot operate properly. The Osc Fail bit latches high and will remain high until cleared by reading at 0Bh. The Osc Fail bit is set after power on or reset. Power is removed on ports with AC disconnect enabled independently of the state of the Osc Fail bit. See AC Disconnect under Applications Information for more details. Bit 4 indicates that V_{EE} has dropped below the V_{EE} UVLO level (typically

REGISTER FUNCTIONS

–26V). Bit 5 signals that the V_{DD} supply has dropped below the V_{DD} UVLO threshold. Bit 7 indicates that the LTC4259 die temperature has exceeded its thermal shutdown (TSD) limit. Thermal shutdown is intended to protect against momentary overload conditions. Junction temperature will exceed 125°C while in thermal shutdown. Continous operation above the specified maximum operating temperature may result in device degredation or failure. The logical OR of bits 1, 4, 5 and 7 appears in the Interrupt register as the Supply Fault bit. See the Misc Config register for information on masking the Osc Fail bit out of the Supply Fault interrupt. The remaining bits in the register are reserved and will always read as 0. The Supply Event bits latch high and will remain high until cleared by reading from address 0Bh.

Supply Event CoR (Address 0Bh): Supply Event Register, Clear on Read. Read this address to clear the Fault Event register. Address 0Bh returns the same data as address 0Ah, and reading address 0Bh clears all bits at both addresses.

Status Registers

Port 1 Status (Address 0Ch): Port 1 Status Register, Read Only. This register reports the most recent detection and classification results for port 1. Bits 0-2 report the status of the most recent detection attempt at the port and bits 4-6 report the status of the most recent classification attempt at the port. If power is on, these bits report the detection/classification status present just before power was turned on. If power is turned off at the port for any reason, all bits in this register will be cleared. See Table 1 for detection and classification status bit encoding.

Port 2 Status (Address 0Dh): Port 2 Status Register, Read Only. See Port 1 Status.

Port 3 Status (Address 0Eh): Port 3 Status Register, Read Only. See Port 1 Status.

Port 4 Status (Address 0Fh): Port 4 Status Register, Read Only. See Port 1 Status.

Power Status (Address 10h): Power Status Register, Read Only. The lower four bits in this register report the switch on/off state for the corresponding ports. The upper four bits, the power good bits, indicate that the drop across the power switch and sense resistor for the corresponding ports is less than 2V, indicating that power start-up is complete

and no current faults are present. The power good bits are latched high and are only cleared when a port is turned off or the LTC4259 is reset.

Pin Status (Address 11h): External Pin Status, Read Only. This register reports the real time status of the external AUTO (Pin 35), AUXIN (Pin 2), and AD0-AD3 (Pins 7-10). The logic state of the AUTO pin appears at bit 0, the AUXIN pin at bit 1, and the AD0-AD3 pins at bits 2-5. The remaining bits are reserved and will read as 0. AUTO affects the initial states of some of the LTC4259 configuration registers at start-up but has no effect after start-up and can be used as a general purpose input if desired, as long as it is guaranteed to be in the appropriate state at start-up.

Configuration Registers

Operating Mode (Address 12h): Operating Mode Configuration, Read/Write. This register contains the mode bits for each of the four ports in the LTC4259. See Table 1 for mode bit encoding. At power-up, all bits in this register will be set to the logic state of the AUTO pin (Pin 35). See Operating Modes in the Applications Information section.

Disconnect Enable (Address 13h): Disconnect Enable Register, Read/Write. The lower four bits of this register enable or disable DC disconnect detection circuitry at the corresponding port. If the DC Discon Enable bit is set the port circuitry will turn off power if the current draw at the port falls below I_{MIN} for more than t_{DIS}. I_{MIN} is equal to V_{MIN}/R_S, where R_S is the sense resistor and should be 0.5Ω for IEEE 802.3af compliance. If the bit is clear the port will not remove power due to low current.

The upper four bits enable or disable AC disconnect on the corresponding port. When a port's AC disconnect bit is set, the LTC4259 senses the impedance of that port by forcing an AC voltage on the port's DETECT pin and measuring the AC current. If the DETECT pin sinks less than I_{ACDMIN} for more than t_{DIS}, the port will turn off power. If the bit is clear, the port will not remove power due to high port impedance (AC current below I_{ACDMIN}).

The DC and AC disconnect signals are ORed together and either sensing method (if they are both enabled) will keep the port powered. A port with neither DC or AC disconnect enabled will not power off automatically when the PD is removed.

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Detect/Class Enable (Address 14h): Detection and Classification Enable, Read/Write. The lower four bits of this register enable the detection circuitry at the corresponding port if that port is in Auto or Semiauto mode. The upper four bits enable the classification circuitry at the corresponding port if that port is in Auto or Semiauto mode. In manual mode, setting a bit in this register will cause the LTC4259 to perform one classification or detection cycle on the corresponding port. Writing to the Detect/Class Restart PB (18h) has the same effect without disturbing the Detect/Class Enable bits for other ports.

Timing Config (Address 16h): Global Timing Configuration, Read/Write. Bits 0-1 program t_{DIS}, the time duration before an undercurrent condition is recognized as a violation of I_{MIN}. Bits 2-3 program t_{ICUT}, the time duration before an overcurrent condition is recognized as a t_{ICUT} fault. Bits 4-5 program t_{START}, the time duration before an overcurrent condition at start-up is considered a t_{START} fault. Note that using t_{ICUT} and t_{START} times other than the default is not compliant with IEEE 802.3af and may double or quadruple the energy dissipated by the external MOSFETs during fault conditions. Bits 6-7 are reserved and should be read/written as 0. See Electrical Characteristics for timer bit encoding.

Misc Config (Address 17h): Miscellaneous Configuration, Read/Write. Bit 5 is the OSC Fail Mask; it is set by default. When the OSC Fail Mask bit is clear, it prevents a failure on the OSCIN pin from setting the OSC Fail bit and causing a Supply Event Interrupt. Setting bit 7 enables the $\overline{INT}$ pin. If this bit is reset, the LTC4259 will not pull down the $\overline{INT}$ pin in any condition nor will it respond to the Alert Response Address. This bit is set by default.

Pushbutton Registers

Note Regarding Pushbutton Registers: "Pushbutton" registers are specialized registers that trigger an event when a 1 is written to a bit; writing a 0 to a bit will do nothing. Unlike a standard read/write register, where setting a single bit involves reading the register to determine its status, setting the appropriate bit in software and writing back the entire register, a pushbutton register allows a single bit to be written without knowing or affecting the status of the other bits in the register. Pushbutton registers are write-only and will return 00h if read.

Det/Class Restart PB (Address 18h): Detection/Classification Restart Pushbutton Register, Write Only. Writing a 1 to any bit in this register will start or restart a single detection or classification cycle at the corresponding port in Manual mode. It can also be used to set the corresponding bits in the Detect/Class Enable register (address 14h) for ports in auto or semiauto mode. The lower 4 bits affect detection on each port while the upper 4 bits affect classification.

Power Enable PB (Address 19h): Power Enable Pushbutton Register, Write Only. The lower four bits of this register set the Power Enable bit in the corresponding Port Status register; the upper four bits clear the corresponding Power Enable bit. Setting or clearing the Power Enable bits via this register will turn on or off the power in any mode except shutdown, regardless of the state of detection or classification. Note that t_{ICUT}, t_{START} and disconnect events (if enabled) will still turn off power if they occur.

The Power Enable bit cannot set if the port has turned off due to a t_{ICUT} or t_{START} fault and the t_{ICUT} timer has not yet counted back to zero. See Applications Information for more information on t_{ICUT} timing.

Clearing the Power Enable bits with this register also clears the detect and fault event bits, the Port Status register, and the Detection and Classification Enable bits for the affected port(s).

Reset PB (Address 1Ah): Reset Pushbutton, Write Only. Bit 4 returns the entire LTC4259 to the power-on reset state; all ports are turned off, the AUTO pin is re-read, and all registers are returned to their power-on defaults. Setting bit 6 releases the Interrupt pin if it is asserted without affecting the Event registers or the Interrupt register. When the $\overline{INT}$ pin is released in this way, the condition causing the LTC4259 to pull the $\overline{INT}$ pin down must be removed before the LTC4259 will be able to pull $\overline{INT}$ down again. This can be done by reading and clearing the event registers or by writing a 1 into bit 7 of this register. Setting Bit 7 releases the Interrupt pin, clears all the Event registers and clears all the bits in the Interrupt register except bit 0 (Power Enable Event). Bits 0-3 reset the corresponding port by clearing the power enable bit, the detect and fault event bits, the status register, and the detection and classification enable bits for that port. Bit 5 is reserved; setting it has no effect.

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APPLICATIONS INFORMATION

OVERVIEW

Over the years, twisted-pair Ethernet has become the most commonly used method for local area networking. The IEEE 802.3 group, the originator of the Ethernet standard, has defined an extension to the standard, known as 802.3af, which allows DC power to be delivered simultaneously over the same cable used for data communication. This promises a whole new class of Ethernet devices, including IP telephones, wireless access points, and PDA charging stations, which do not require additional AC wiring or external power transformers, a.k.a. "wall warts." With about 13W of power available, small data devices can be powered by their Ethernet connection, free from AC wall outlets. Sophisticated detection and power monitoring techniques prevent damage to legacy data-only devices, while still supplying power to newer, Ethernet-powered devices over the twisted-pair cable.

A device that supplies power is called Power Sourcing Equipment (PSE); a device that draws power from the wire is called a Powered Device (PD). A PSE is typically an Ethernet switch, router, hub, or other network switching equipment that is commonly found in the wiring closets where cables converge. PDs can take many forms: digital IP telephones, wireless network access points, PDA or notebook computer docking stations, cell phone chargers, and HVAC thermostats are examples of devices that can draw power from the network.

A PSE is required to provide a nominal 48V DC between either the signal pairs or the spare pairs (but not both) as shown in Figure 11. The power is applied as a voltage between two of the pairs, typically by powering the center-taps of the isolation transformers used to couple the differential data signals to the wire. Since Ethernet data is transformer coupled at both ends and is sent differentially, a voltage difference between the transmit pairs and the receive pairs does not affect the data. A 10/100base-T Ethernet connection only uses 2 of the 4 pairs in the cable. The unused or spare pairs can be powered directly, as shown in Figure 11, without affecting the data. However, 1000base-T uses all 4 pairs and power must be connected to the transformer center taps if compatibility with 1000base-T is required.

The LTC4259 provides a complete solution for detection and powering of PD devices in an IEEE 802.3af compliant system. The LTC4259 consists of four independent ports, each with the ability to detect, classify, and provide isolated −48V power to a PD device connected to it. The LTC4259 senses removal of a PD with IEEE 802.3af compliant AC or DC methods and turns off −48V power when the PD is removed. A global control circuit takes care of system configuration and timing, and uses an I^2C interface to communicate with the host system.
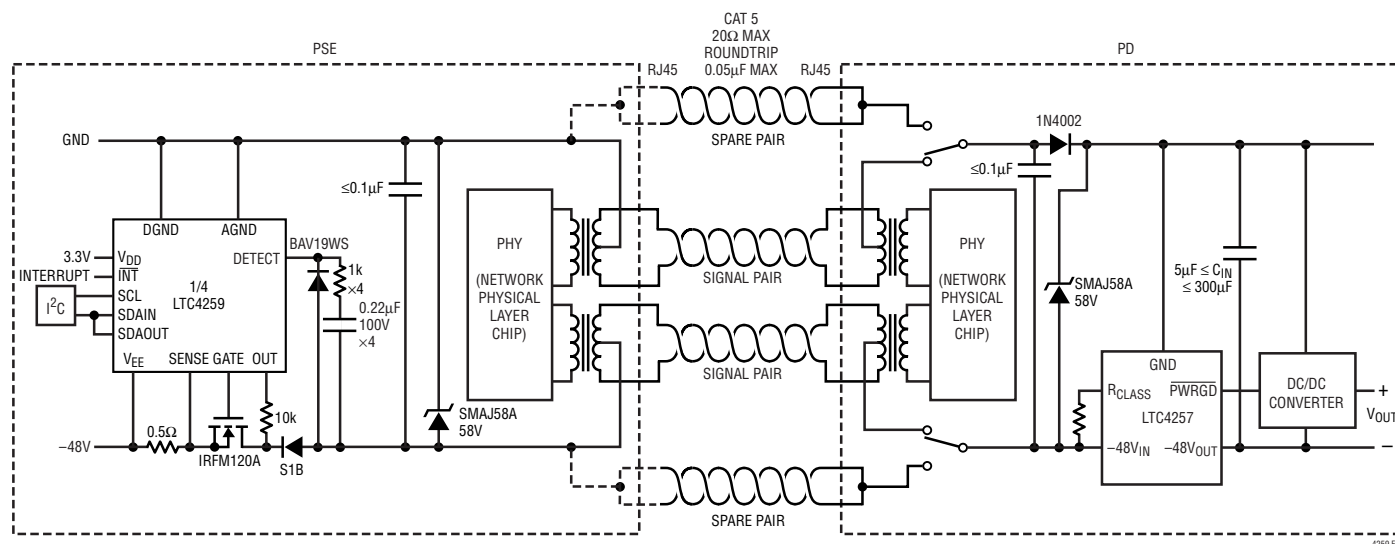

Figure 11. System Diagram

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OPERATING MODES

Each LTC4259 port can operate in one of four modes: Manual, Semiauto, Auto or Shutdown. The operating mode for a port is set by the appropriate bits in the Operating Mode register. The LTC4259 will power up with all ports in Shutdown mode if the external AUTO pin is tied low; if AUTO is high, all ports will wake up in Auto mode. The operating mode can be changed at any time via the I^{2}C interface, regardless of the state of the AUTO pin.

• In Manual mode, a port will wait for instructions from the host system before taking any action. It will run single detection or classification cycles when commanded, and will report results in the Port Status registers. When the host system decides it is time to turn on or off power to a port, it can do so by setting the appropriate Power On/Off bits in the Power Enable PB register regardless of the current status of detection or classification.

• In Semiauto mode, the port will continuously attempt to detect and classify a PD device attached to the link. It will report this information in its Port Status register, and wait for the host system to set the appropriate Power On bit in the Power Enable PB register before applying power to the port.

• In Auto mode, the port will detect and classify a PD device connected to it, then immediately turn on the power if detection was successful regardless of the result of classification.

• In Shutdown mode, the port is disabled and will not detect or power a PD. Also, the detect and fault event bits, status bits and enable bits for the port are reset to zero.

Regardless of which mode it is in, the LTC4259 will remove power automatically from any port that generates a t_{START} or t_{ICUT} overcurrent fault event (see t_{ICUT} Timing and t_{START} Timing sections). It will also automatically remove power from any port that generates a disconnect event if the appropriate Disconnect Enable bit is set in the Disconnect Enable register. The host controller may also remove power at any time by setting the appropriate Power Off bit in the Power Enable PB register.

Power-On RESET

At turn-on or any time the LTC4259 is reset (either by pulling the RESET pin low or writing to the global Reset All bit), all the ports turn off and all internal registers go to a predefined state, shown in Table 1.

Several of the registers assume different states based on the state of the AUTO pin at reset. The default states with AUTO high allow the LTC4259 to detect and power up a PD in Automatic mode, even if nothing is connected to the I^{2}C interface.

SIGNATURE DETECTION

The IEEE defines a specific pair-to-pair PD signature resistance that identifies a device that can accept Power over Ethernet in accordance with the 802.3af specification. When the channel voltage is below 10V, an 802.3af compliant PD will have a 25k signature resistance. Figure 12 illustrates the relationship between the PD signature resistance (white box from 23.75k to 26.25k) and required resistance ranges the PSE must accept (white box) and reject (gray boxes). According to the 802.3af specification, the PSE may or may not accept resistances in the two ranges of 15k to 19k and 26.5k to 33k. Note that the black box in Figure 12 represents the 150Ω pair-to-pair termination used in legacy 802.3 devices like a computer's network interface card (NIC) that cannot accept power.
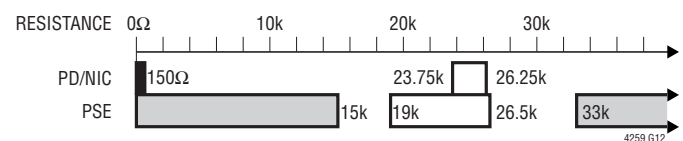

Figure 12. IEEE 802.3af Signature Resistance Ranges

The LTC4259 checks for the signature resistance by forcing two test currents on the wire in sequence and measuring the resulting voltages. It then subtracts the two V-I points to determine the resistive slope while removing voltage offset caused by any series diodes or current offset caused by leakage at the port (see Figure 13). The LTC4259 will typically accept any PD resistance between
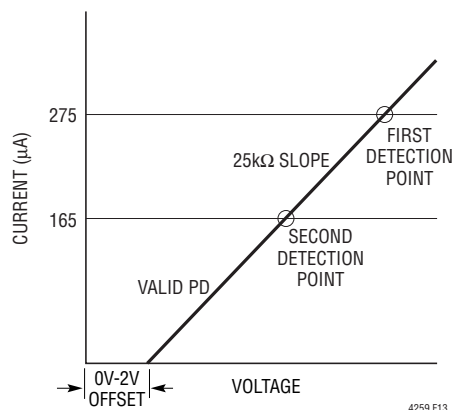
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Figure 13. PD Detection

17k and 29k (between 19k and 26.5k guaranteed) as a valid PD and report Detect Good (100 binary) in the Detect Status bits (bits 2 through 0) of the corresponding Port Status register. Values outside this range, including open and short circuits, are also reported in the Detect Status bits. Refer to Table 1 for a complete decoding of the Detect Status bits.

The first test point is taken by forcing a test current into the port, waiting a short time to allow the line to settle and measuring the resulting voltage. This result is stored and the second current is applied to the port, allowed to settle and the voltage measured. Each point takes 100ms to measure, and an entire detection cycle takes 200ms.

The port's operating mode controls if and when the LTC4259 runs a detection cycle. In manual mode, the port will sit idle until a Restart Detection (register 18h) command is received. It will then run a complete 200ms detection cycle on the selected port, report the results in the Detect Status bits in the corresponding Port Status register and return to idle until another command is received. In Semiauto mode, the LTC4259 autonomously

tests valid PDs connected to the ports but it will not apply power until instructed to do so by the host controller. It repeatedly queries the port every 320ms and updates the Detect Status bits at the end of each cycle. If a Detect Good is reported, it will advance to the classification phase and report that result in the Port Status register. Until instructed to do otherwise, the LTC4259 will continue to repeat detection on the port. Behavior in Auto mode is similar to Semiauto; however, after a Detect Good is reported, the LTC4259 performs the classification phase and then powers up the port without further intervention.

The signature detection circuitry is disabled when the port is in Shutdown mode, powered up or the corresponding Detect Enable bit is cleared.

CLASSIFICATION

A PD has the option of presenting a "classification signature" to the PSE to indicate how much power it will draw when powered up. This signature consists of a specific constant current draw when the PSE port voltage is between 15.5V and 20.5V, with the current level indicating the power class to which the PD belongs. Per the IEEE 802.3af specification, the LTC4259 identifies the five classes of PD listed in Table 2. Note that class 4 is presently specified by the IEEE as reserved for future use but it is intended to be used with PDs that digitally communicate additional requirements over the Ethernet interface after being powered. Figure 14 shows a PD load line, starting with the shallow slope of the 25k signature resistor below 10V then drawing the proper current for class 3 between 15V and 20V. The LTC4259's load line for classification is also shown in Figure 14. It has low impedance until current limit at 65mA (typ).

Table 2. IEEE 802.3af Powered Device Classes

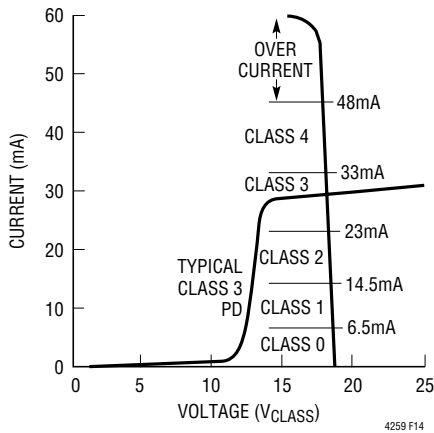| IEEE 802.3fa CLASS	CLASSIFICATION CURRENT	MAXIMUM PD POWER	CLASS DESCRIPTION
0	0mA to 4mA	12.95W	Unknown PD Power, PD Does Not Implement Classification
1	9mA to 12mA	3.84W	Low Power PD
2	17mA to 20mA	6.49W	Medium Power PD
3	26mA to 30mA	12.95W	High or Full Power PD
4	36mA to 44mA	12.95W	Reserved, Power as Class 0

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Figure 14. PD Classification

The LTC4259 will classify a port immediately after a successful detection cycle in Semiauto or Auto modes, or when commanded in Manual mode. It measures the PD classification signature current by applying 18V (typ) to the port and measuring the resulting current. It reports the detected class in the Class Status bits in the corresponding Port Status register. Note that in Auto mode, the port will power up regardless of which class is detected.

The classification circuitry is disabled when the port is in Shutdown mode, powered up, or the corresponding Class Enable bit is cleared.

POWER CONTROL

The primary function of the LTC4259 is to control the delivery of power to the PSE port. It does this by controlling the gate drive voltage of an external power MOSFET while monitoring the current via a sense resistor and the output voltage at the OUT pin. This circuitry serves to couple the raw isolated −48V input supply to the port in a controlled manner that satisfies the PD's power needs while minimizing disturbances on the −48V backplane.

Gate Currents

Once the decision has been made to turn on the power to a port, the LTC4259 uses a 50µA current source to pull up on the GATE pin. Under normal power-up circumstances,

the MOSFET gate will charge up quickly to V_T (the MOSFET threshold voltage), the MOSFET current will rise quickly to the current limit level and the GATE pin will be servoed to maintain the proper I_{INRUSH} charging current. When output charging is complete, the MOSFET current will fall and the GATE pin will be allowed to continue rising to fully enhance the MOSFET and minimize its on resistance. The final V_{GS} is nominally 13V. When a port is turned off, a 50µA current source pulls down on the GATE pin, turning the MOSFET off in a controlled manner.

No External Capacitors

No external capacitors are required on the GATE pins for active current limit stability, lowering part count and cost. This also allows the fastest possible turn-off under severe overcurrent conditions, providing maximum safety and protection for the MOSFETs, load devices and board traces. Connecting capacitors to the external MOSFET gates will adversely affect the LTC4259's ability to respond to a shorted port.

Inrush Control

When the LTC4259 turns on a port, it turns on the MOSFET by pulling up on the gate. The LTC4259 is designed to power up the port in current limit, limiting the inrush current to I_{INRUSH}.

The port voltage will quickly rise to the point where the PD reaches its input turn-on threshold and begins to draw current to charge its bypass capacitance, slowing the rate of port voltage increase.

The 802.3af specification lists two separate maximum current limits, I_{LIM} and I_{INRUSH}. Because they have identical values, the LTC4259 implements both as a single current limit using V_{LIM} (described below). Their functions are differentiated through the use of t_{ICUT} and t_{START}, respectively (see t_{ICUT} Timing and t_{START} Timing sections). To maintain consistency with the specification, the I_{INRUSH} term is used when referring to an initial t_{START} power-up event.

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Dual-Level Current Limit

A PD is permitted to draw up to 350mA continuously and up to 400mA for 50ms. The LTC4259 has two corresponding current limit thresholds, I_{CUT} (350mA to 400mA, 375mA typ) and I_{LIM} (400mA to 450mA, 425mA typ). These are given by the equations:

$$I_{CUT} = V_{CUT}/R_S, \quad I_{LIM} = V_{LIM}/R_S$$

R_S is the sense resistor and should be 0.5Ω for IEEE 802.3af compliance. Two 1% 1Ω thick-film resistors in parallel may be used to minimize cost. While the LTC4259 allows the port current to exceed I_{CUT} for a limited time period (see t_{ICUT} timing below), it does not allow the current to exceed I_{LIM}. The current limit circuit monitors the port current by monitoring the voltage across the sense resistor and reduces the MOSFET gate voltage as needed to keep the current at or below I_{LIM}. When the current drops below I_{LIM}, the gate voltage is restored to the full value to keep the MOSFET resistance to a minimum.

t_{ICUT} Timing

Whenever more than $I_{CUT} = V_{CUT}/R_S$ flows through a port, the port's sense voltage is above V_{CUT} and the t_{ICUT} timer counts up. If the sense voltage is still above V_{CUT} when the t_{ICUT} timer expires, the LTC4259 will turn off the power to the port immediately and set the appropriate t_{ICUT} Fault bit in register 06h/07h. The t_{ICUT} timer duration can be programmed via register 16h, bits 3 and 2 (Table 1).

The t_{ICUT} timer is an up/down counter that is designed to protect the external MOSFET from thermal stress caused by operating in current limit for an extended duration. The counter counts up whenever the current is above I_{CUT} and counts down at 1/16th the rate when it is not. The counter will bottom out at zero to prevent underflow. Full count indicates that the t_{ICUT} timer has expired and the port will be turned off.

This count up/count down behavior creates duty cycle protection, preventing intermittent current limit faults from causing cumulative thermal stress in the MOSFET. If the port enters current limit but then exits before the timer expires, the count will decrease slowly, giving the I_{CUT} timer a headstart with a repeated fault unless the repeat interval is infrequent (less than 6.3% duty cycle typ).

If the t_{ICUT} timer expires and causes the port to shut off, the timer will continue to run, counting down at the slow 1/16th rate and preventing the port from being repowered until the count returns to zero. This protects the MOSFET from damage due to a faulty PD that may still have a valid signature, or from errant software that repeatedly writes to the Power On bit.

The port will not repower until a valid detect occurs after the count returns to zero in auto mode or the power on bit is written to after the count returns to zero. Writing to the power on bit before the count returns to zero has no effect.

t_{START} Timing

To distinguish between normal turn-on current limit behavior and current limit faults which occur after power-up is complete, the LTC4259 starts a timer (the t_{START} timer) whenever a power-up sequence begins.

The t_{START} timer serves three functions. First and foremost, it allows the user to specify a different current limit timeout (t_{START} instead of t_{ICUT}) during turn-on (current limit duty cycle protection remains functional). Second, the DC disconnect timer is disabled during this period and can only begin counting up after the t_{START} timer has expired. Together, these two features let the PD draw the maximum current I_{INRUSH} to charge its input capacitance, boot up and begin drawing the minimum load without triggering a t_{START} fault. Finally, if the device is in current limit for the entire t_{START} period, a t_{START} fault will be generated instead of a t_{ICUT} fault. This can be useful for tracking down the cause of a current fault.

As long as the PD draws less than I_{CUT} at the end of t_{START} and begins drawing the minimum current within t_{DIS} after t_{START} expires (if DC disconnect is enabled) no faults will be indicated.

The t_{START} timer also implements duty cycle protection and its duration can be programmed via register 16h, bits 5 and 4 (Table 1).

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Foldback

Foldback is designed to limit power dissipation in the MOSFET during short-circuit conditions and during power-up. At low port output voltages, the voltage across the MOSFET is high, and power dissipation will be large if significant current is flowing. Foldback monitors the port output voltage and reduces the V_{LIM} current limit level linearly from its full value (212.5mV typ) at a port voltage of 18V to approximately 1/7th of the full value (30mV typ) at a port voltage of 0V. With 0.5Ω sense resistors, this limits the short-circuit current to 60mA (typ) instead of the full 425mA (typ) current limit. The V_{CUT} overcurrent threshold is also lowered to ensure that the current limit fault timer runs while the port is in foldback current limit.

Short-Circuit Protection

If a port is suddenly shorted out, the MOSFET power dissipation can rise to very high levels, jeopardizing the MOSFET even before the normal current limit circuit can respond. A separate short-circuit current limit circuit watches for significant overcurrent events (V_{SENSE} >275mV, >550mA with a 0.5Ω sense resistor) and pulls the GATE pin down immediately if such an event occurs, shutting off the MOSFET in less than 1μs (with no external capacitor on GATE). Approximately 100μs later, GATE is allowed to rise back up and the normal current limit circuit will take over, allowing I_{LIM} current to flow and causing the t_{ICUT} timer to count up. During a short circuit, I_{LIM} will be reduced by the foldback feature to 1/7th of the nominal value.

Choosing External MOSFETs

Power delivery to the ports is regulated with external power MOSFETs. These MOSFETs are controlled as previously described to meet the IEEE 802.3af specification. Under normal operation, once the port is powered and the PD's bypass capacitor is charged to the port voltage, the external MOSFET dissipates very little power, at most FET $R_{ON} \cdot (350mA)^2$. This suggests that a small MOSFET is adequate for the job. Unfortunately, other requirements of the IEEE 802.3af mandate a FET capable of dissipating

significant power. When the port is being powered up, the port voltage must reach 30V or more before the PD turns on. The port voltage can then drop to 0V as the PD's bypass capacitor is charged. According to the IEEE, the PD can directly connect a 180μF capacitor to the port and the PSE must charge that capacitor with a current limit of 400mA to 450mA for at least 50ms.

An even more extreme example is a noncompliant PD that provides the proper signature during detection but then behaves like a low valued resistor, say 50Ω, in parallel with a 1μF capacitor. When the PSE has charged this noncompliant PD up to 20V, the 50Ω resistor will draw 400mA (the minimum IEEE prescribed I_{LIM} current limit) keeping the port voltage at 20V for the remainder of t_{START}. The external MOSFET sees 24V to 37V V_{DS} at 400mA to 450mA, dissipating 9.6W to 16.7W for 60ms (typ). The LTC4259 implements foldback to reduce the current limit when the MOSFET V_{DS} is high; see the Foldback section and the Typical Performance curves. Without foldback, the MOSFET could see as much as 25.7W for 60ms (typ) when powering a shorted or a noncompliant PD with only a few ohms of resistance. Thanks to foldback, the MOSFET sees a maximum 18W for the duration of t_{START}.

The LTC4259's duty cycle protection enforces 15 times longer off time than on time, preventing successive attempts to power a defective PD from damaging the MOSFET. System software can enforce even longer wait times. When the LTC4259 is operated in semiauto or manual mode—described in more detail under Operating Modes—it will not power on a port until commanded to do so by the host controller. By keeping track of t_{START} and t_{ICUT} faults, the host controller can delay turning on the port again after one of these faults even if the LTC4259 reports a Detect Good. In this way the host controller implements a MOSFET cooling off period which may be programmed to protect smaller MOSFETs from repeated thermal cycling. The LTC4259 has built-in duty cycle protection for t_{ICUT} and t_{START} (see t_{ICUT} Timing and t_{START} Timing sections) that is sufficient to protect the MOSFETs shown in Figure 1.

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Before designing a MOSFET into your system, carefully compare its safe operating area (SOA) with the worst case conditions (like powering on a defective PD) the device will face. Using transient suppressors, polyfuses and extended wait times after disconnecting a PD are effective strategies to reduce the extremes applied to the external MOSFETs.

Surge Suppressors and Circuit Protection

IEEE 802.3af Power over Ethernet is a challenging Hot Swap application because it must survive the (probably unintentional) abuse of everyone in the building. While hot swapping boards in a networking or telecom card cage is done by a trained technician or network administrator, anyone in the building can plug a device into the network. Moreover, in a card cage the physical domain being powered is confined to the card cage. With Power over Ethernet, the PSE supplies power to devices up to 100 meters away. Ethernet cables could potentially be cut, shorted together, and so on by all kinds of events from a contractor cutting into walls to someone carelessly sticking a screwdriver where it doesn't belong. Consequently the Power over Ethernet power source (PSE) must be designed to handle these events.

The most dramatic of these is shorting a powered port. What the PSE sees depends on how much CAT-5 cable is between it and the short. If the short occurs on the far end of a long cable, the cable inductance will prevent the current in the cable from increasing too quickly and the LTC4259's built-in short-circuit protection will take control of the situation and turn off the port. Some energy is stored in the cable, but the transient suppressor on the port clamps the port voltage when the cable inductance flies back after the MOSFET is turned off. Because the cable only had 600mA or so going through it, an SMAJ58A or other device can easily control the port voltage during flyback. With no cable connected at all, a powered port shorted at the PSE's RJ-45 connector can reach high current levels before the port is shut down. There is no cable inductance to store energy so once the port is shut down the situation is under control.

In the intermediate case things get exciting. A short—hence low inductance—piece of CAT-5 will not limit the rapid increase of current when the port is shorted. Even though the LTC4259 short-circuit shutdown is fast, the cable may have many amps flowing through it before the MOSFET can be turned off. Due to the high current, this short piece of cable flies back with significant energy behind it and must be controlled by the transient suppressor. Choosing a surge suppressor that will not develop more than a few volts of forward voltage while passing more than 10A is important. A positive port voltage may forward bias the detect diode (D_{DETn}), bringing the LTC4259's DETECTn pin positive as well and engaging the DETECTn clamps. This will generally not damage the LTC4259 but it can cause the LTC4259 to reset. When it resets, the LTC4259 signals an interrupt, alerting the host controller which can then return the LTC4259 to normal operating mode.

A substantial transient surge suppressor can typically protect the LTC4259 and the rest of the PSE from these faults. Placing a polyfuse between the RJ-45 connector and the LTC4259 and its associated circuitry can provide additional protection. Connecting the transient surge suppressor to the RJ-45 side of the fuse allows the transient surge suppressor to control port voltage even when the polyfuse is open. To meet safety requirements, place a polyfuse in the ground leg of the PSE's output.

DC DISCONNECT

DC disconnect watches the sense resistor voltage whenever the power is on to make sure that the PD is drawing the minimum specified current. The disconnect timer counts up whenever port current is below 5mA to 10mA, 7.5mA typ. If the t_{DIS} timer runs out, the corresponding port will be turned off and the disconnect bit in the fault register will be set. If the undercurrent condition goes away before the t_{DIS} timer runs out, the timer will reset. The timer will start counting from the beginning if the undercurrent condition occurs again. The undercurrent circuit includes a glitch filter to filter out noise.

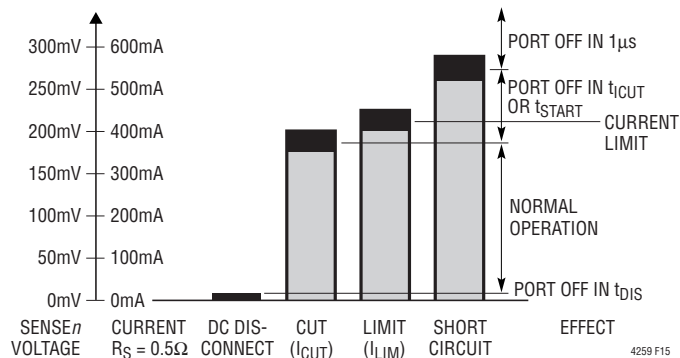# APPLICATIONS INFORMATION

Figure 15. LTC4259 Current Sense and Limits

The DC disconnect feature can be disabled by clearing the corresponding DC Discon Enable bits in the Disconnect register (13h). The t_{DIS} timer duration can be programmed by bits 1 and 0 of register 16h.

The LTC4259 implements a variety of current sense and limit thresholds to control current flowing through the port. Figure 15 is a graphical representation of these thresholds and the action the LTC4259 takes when currrent crosses the thresholds.

AC DISCONNECT

AC disconnect is an alternate method of sensing the presence or absence of a PD by monitoring the port impedance. The LTC4259 forces a signal, amplified from the OSCIN pin, out of the DETECT pins and onto the Power over Ethernet connection. It calculates the connection impedance from ohm's law, $Z_{PORT} = V_{AC}/I_{AC}$. Like DC disconnect, the AC disconnect sensing circuitry controls the disconnect timer. When the connection impedance rises (AC current falls below I_{ACDMIN}) due to the removal of the PD, the disconnect timer counts up. If the impedance remains high (AC current remains below I_{ACDMIN}), the disconnect timer counts to t_{DIS}, the port is turned off and the port's disconnect bit in the Fault Register is set. If connection impedance falls (AC current rises above I_{ACDMIN}) before maximal count of the disconnect timer, the timer resets and the port remains powered.

Like DC disconnect, AC disconnect can also be disabled by clearing the corresponding AC Discon Enable bits in the Disconnect register (13h). AC disconnect is also affected by the t_{DIS} duration programmed in register 16h.

Unlike DC disconnect, AC disconnect has no continuous time output to the timer. Rather, AC disconnect will reset the timer once every cycle, $1/f_{OSCIN}$, of the OSCIN signal if the port draws more than I_{ACDMIN} during that period. Because of this behavior, the time to turn off the port after PD removal, t_{DIS}, may be up to one cycle of OSCIN ($1/f_{OSCIN}$) shorter than the delay programmed with the t_{DIS1} and t_{DIS0} bits. Note that AC disconnect and DC disconnect signals that reset the t_{DIS} timer are ORed together. Thus on a channel where both disconnect modes are enabled, either disconnect sensing method can keep the port powered even if the other reports that there is no PD connected.

The AC disconnect circuitry senses the port and Power over Ethernet connection from the DETECT pins. Connect a 0.22μF 100V X7R capacitor (C_{DET}) and a 1k resistor (R_{DET}) from the port's DETECT pin to the port's output as shown in Figure 16. This provides an AC path for sensing the channel impedance. The 1k resistor, R_{DET}, limits current flowing through this path during port power on and power off.

Sizing of capacitors is critical to ensure proper function of AC disconnect. C_{PSE} (Figure 16) controls the connection impedance on the PSE side. Its capacitance must be kept low enough for AC disconnect to be able to sense the PD. For operation near 100Hz, use a C_{PSE} of 0.1μF or less. On the other hand, C_{DET} has to be large enough to pass the signal at the frequency of OSCIN. For $f_{OSCIN} \approx 100$Hz, use at least a 0.22μF 100V X7R capacitor. The sizes of C_{PSE}, C_{DET}, R_{DET} and the frequency, f_{OSCIN}, are chosen to create an economical, physically compact and functionally robust system. Moreover, the complete Power over Ethernet AC disconnect system (PSE, transformers, cabling, PD, etc.) is complex; deviating from the recommended values of C_{DET}, R_{DET} and C_{PSE} is discouraged. Contact the LTC Applications department for additional support.

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When choosing C_{DET} and C_{PSE}, carefully consider voltage derating of the capacitors. Capacitors built around an X7R dielectric will have about 60% of the specified capacitance at their rated voltage. Operated at half their rated voltage, X7R capacitors exhibit more than 80% of their specified capacitance. With other ceramic dielectrics commonly used in 50V and 100V chip capacitors, capacitance falls much more dramatically with voltage. At their rated voltage, Y5V or Z5U capacitors exhibit less than 30% of their zero-bias capacitance. In order to produce the desired capacitance at the operating bias, 100V X7R capacitors should be used with the LTC4259.

As illustrated in Figure 17, the Power over Ethernet connection between the PSE and PD includes a large amount of capacitance. Cable capacitance is particularly troubling because CAT-3 and CAT-5 pair-to-pair capacitance is not tightly specified by the IEEE 802.3 standard or well controlled by cable manufacturers. Considering that patch panels, additional connectors, old wiring, etc. are likely to be placed between the PSE and PD, pair-to-pair capacitance is a pretty nebulous quantity. Consequently, the impedance of the cable capacitance at the frequency used for AC disconnect can be a cause for concern. Assumimg that f_{OSCIN} is 100Hz, the 0.1µF of C_{PSE} plus 0.05µF of cable capacitance gives a port impedance of 10k at 100Hz. The PD AC signature resistance is about 25k. Connecting a PD with the maximum allowed resistance of 26.25k brings the connection impedance to about 8k. The presence of a PD only makes a 20% reduction in the port impedance. With some methods used for AC disconnect, cable capacitance can fool the PSE into keeping the port powered. Fortunately, the LTC4259 has a solution to this problem. When
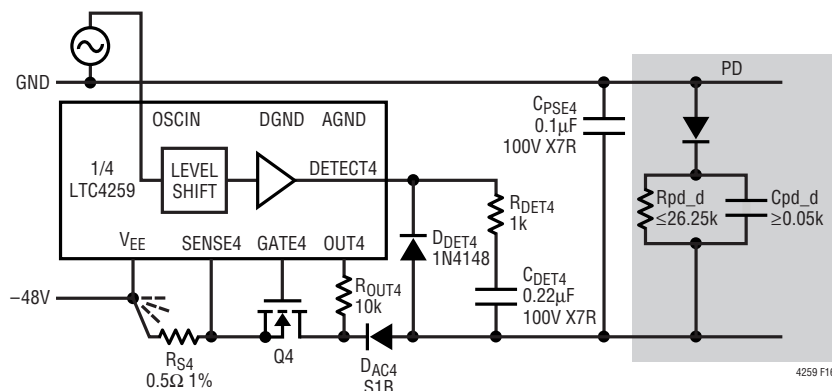

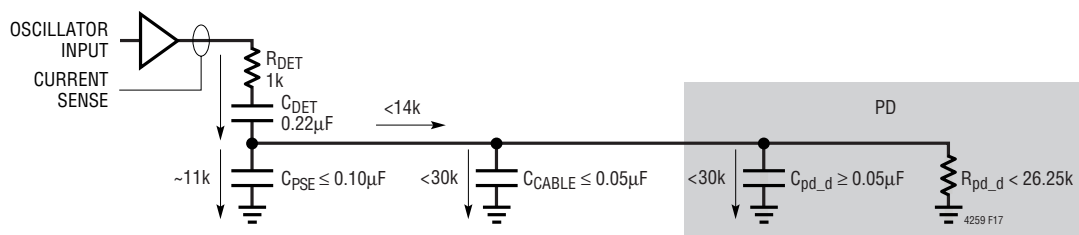**Figure 16. AC Disconnect Single Channel Application Circuit**

Figure 17. Simplified AC Disconnect Circuit with Impedances at 100Hz

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the OSCIN pin is driven with either a sine wave or a smoothed trapezoid wave, the LTC4259 is able to distinguish between capacitive impedance and resistive impedance on the Power over Ethernet connection. The cable capacitance has to really get out of hand (about 0.5μF, which is an order of magnitude greater than worst case for a long CAT-3 or CAT-5 cable) before the LTC4259 has any trouble.

OSCIN Input and Oscillator Requirements

AC disconnect depends on an external oscillator source applied to the OSCIN pin. The LTC4259 measures channel impedance by applying an amplified version of the OSCIN signal to the port's DETECT pin (see Figure 16). The oscillator should be well-controlled because errors in this signal become errors in the measured channel impedance. As shown in Figure 17, the load being sensed by AC disconnect has a resistive and a large reactive component. Current through the PD's signature resistor depends on the amplitude of the AC signal while current into the capacitors depends on the slew rate; $I = C \cdot dV/dt$. Consequently, the LTC4259 is sensitive to the amplitude and slew rate of the OSCIN signal, but is more tolerant of frequency and offset errors. Internal limits prevent the LTC4259 from being adversely affected by OSCIN signals with excessive amplitude.

There are many ways to build oscillators with controlled amplitudes and slew rates, especially since the frequency of the oscillator does not have to be well-controlled. An example oscillator circuit will be provided in a later version of this data sheet. Contact the LTC Applications department for additional oscillator circuits.

Slew rates between 0.5V/ms and 1.2V/ms are required with the recommended values of C_{DET}, R_{DET} and C_{PSE}. The LTC4259 will work with other slew rates if C_{DET}, R_{DET} and C_{PSE} are resized. As alluded to previously, AC disconnect is complicated and redesigning for different component sizes is a difficult task. Keep in mind that the IEEE 802.3af specification places upper limits of 100V/ms on the slew

rate and 500Hz on the frequency of the AC signal at the port. Voltage gain, A_{VACD}, from OSCIN to DETECTn increases the slew rate by the voltage gain. Since A_{VACD} has a maximum absolute value of 3.3V/V (±3V typ), the slew rate at the OSCIN pin must be less than 30V/ms.

The LTC4259's OSCIN input amplifier will accept signals between DGND – 0.3V and V_{DD} + 0.5V. This amplifier has a gain of –1 and is referenced to 1.2V above DGND. An OSCIN voltage greater than 2.2V will cause the amplifier's output to clip against DGND. Clipping will not affect the performance of AC disconnect until the clipping becomes so severe that even the midrange (where the controlled slew rate occurs) of the signal is clipped. Keep the midrange or average voltage of the OSCIN signal below 1.5V to avoid severe clipping. OSCIN signals below DGND can interact with the ESD protection circuitry on the pin and are therefore discouraged. Also, meeting the IEEE 802.3af specification for maximum AC amplitude on the port just after the PD is removed can depend on the OSCIN input peak-to-peak amplitude. Clipping by LTC4259's OSCIN input circuitry will generally ensure that this specification is met. Note that under normal operation, the AC disconnect output on the DETECTn pin will have an amplitude near 6V peak-to-peak. The combination of R_{DET}, C_{DET} and C_{PSE} attenuate the signal so half this amplitude is seen at the port when the channel is powered and the PD has just been removed. When the PD is still connected there will be almost no AC amplitude on the port.

The LTC4259 monitors Pin 36 for the presence of an oscillating signal. If no signal is present and the Osc Fail Mask bit is set, then Osc Fail (bit 1 of the Supply Event register) is set, triggering an interrupt. As the LTC4259's AC disconnect circuitry self-checks the OSCIN signal, the Osc Fail bit is intended as a fault indicator to alert the PSE host controller. Beyond triggering an interrupt, the Osc Fail bit has no effect. The Osc Fail bit being clear indicates that the OSCIN signal goes below 0.6V and above 1.8V at least once every 250ms. It does not necessarily guarantee that AC disconnect will function properly. However, AC

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disconnect itself is a more thorough test of the OSCIN signal. When the OSCIN signal is either absent or corrupted, powered channels with AC disconnect enabled (and DC disconnect not enabled) will automatically disconnect of their own accord in time t_{DIS}. After the LTC4259 is reset (by power on, Reset All bit or the $\overline{RESET}$ pin) the Osc Fail bit is set. Once the Osc Fail bit is cleared, it will only be set by an invalid signal on the OSCIN pin or another reset.

SERIAL DIGITAL INTERFACE

The LTC4259 communicates with a host (master) using the standard 2-wire interface as described in the SMBus Specification Version 2.0 (available at http://smbus.org). The SMBus is an extension of the I²C bus, and the LTC4259 is also compatible with the I²C bus standard. The Timing Diagrams show the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 SMBus accelerator, are required on these lines. If the SDA and SCL pull-ups are absent, not connected to the same positive supply as the LTC4259's V_{DD} pin, or are not activated when the power is applied to the LTC4259, it is possible for the LTC4259 to see a START condition on the I²C bus. The interrupt pin ($\overline{INT}$) is only updated between I²C transactions. Therefore if the LTC4259 sees a START condition when it powers up because the SCL and SDA lines were left floating, it will not assert an interrupt (pull $\overline{INT}$ low) until it sees a STOP condition on the bus. In a typical application the I²C bus will immediately have traffic and the LTC4259 will see a STOP so soon after power up that this momentary condition will go unnoticed.

Isolating the Serial Digital Interface

IEEE 802.3af requires that network segments be electrically isolated from the chassis ground of each network interface device. However, the network segments are not required to be isolated from each other provided that the segments are connected to devices residing within a single building on a single power distribution system.

For simple devices such as small powered Ethernet switches, the requirement can be met by using an isolated power supply to power the entire device. This implementation can only be used if the device has no electrically conducting ports other than twisted-pair Ethernet. In this case, the SDAIN and SDAOUT pins of the LTC4259 can be connected together to act as a standard SDA pin.

If the device is part of a larger system, contains serial ports, or must be referenced to protective ground for some other reason, the Power over Ethernet subsystem including the LTC4259s must be isolated from the rest of the system. The LTC4259 includes separate pins (SDAIN and SDAOUT) for the input and output functions of the bidirectional data line. This eases the use of optocouplers to isolate the data path between the LTC4259s and the system controller. Figure 18 shows one possible implementation of an isolated interface. The SDAOUT pin of the LTC4259 is designed to drive the inputs of an optocoupler directly, but a standard I²C device typically cannot. U1 is used to buffer I²C signals into the optocouplers from the system controller side. Schmitt triggers must be used to prevent extra edges on transitions of SDA and SCL.

Bus Addresses and Protocols

The LTC4259 is a read-write slave device. The master can communicate with the LTC4259 using the Write Byte, Read Byte and Receive Byte protocols. The LTC4259's primary serial bus address is $(010A_3A_2A_1A_0)$b, as designated by pins AD3-AD0. All LTC4259s also respond to the address (0110000)b, allowing the host to write the same command into all of the LTC4259s on a bus in a single transaction. If the LTC4259 is asserting (pulling low) the $\overline{INT}$ pin, it will also acknowledge the Alert Response Address (0001100)b using the receive byte protocol.
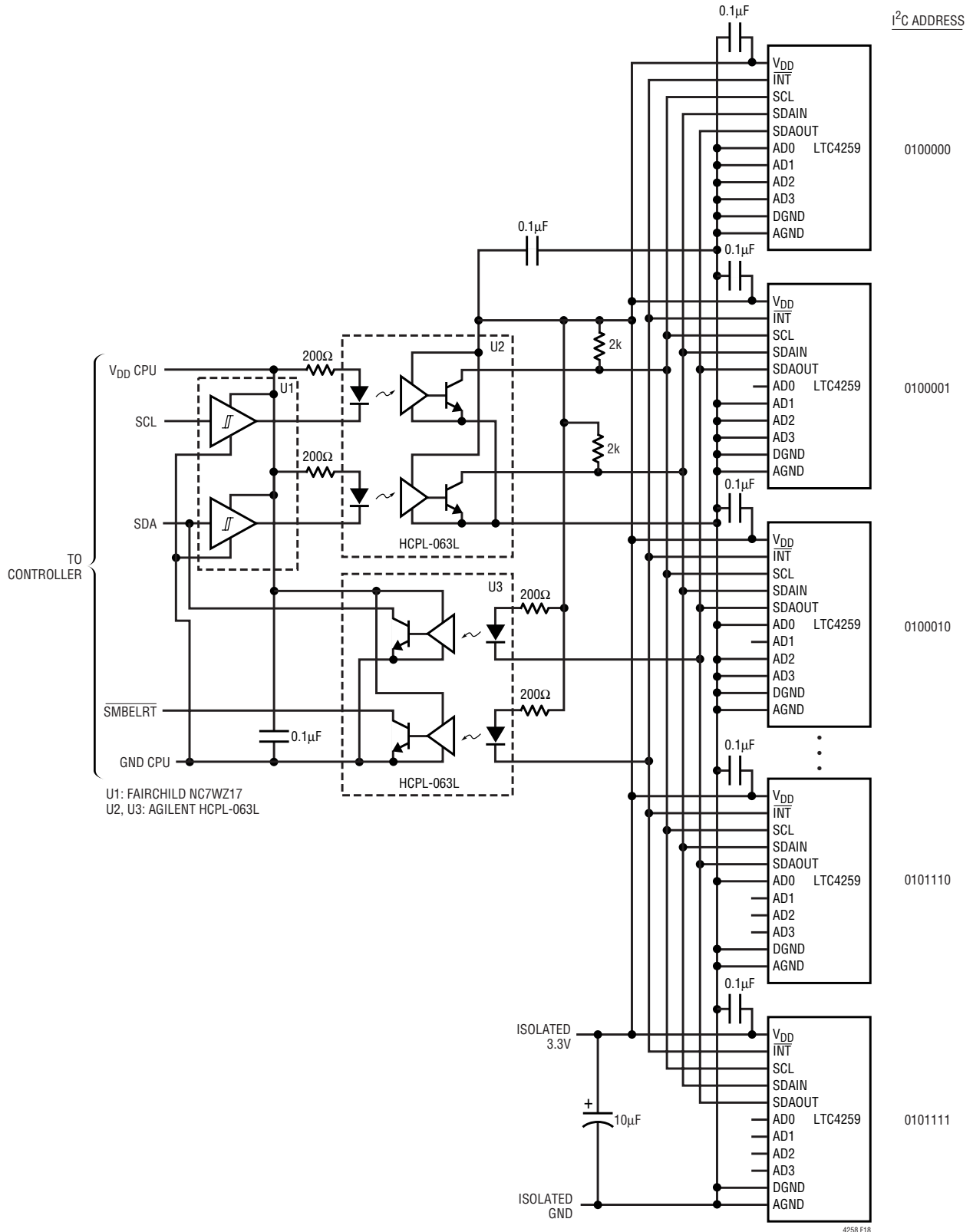
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Figure 18. Optoisolating the I²C Bus

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The START and STOP Conditions

When the bus is idle, both SCL and SDA must be high. A bus master (typically the host system) signals the beginning of a communication to a slave device (like the LTC4259) by transmitting a START condition. A START condition is generated by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition. A STOP condition is generated by transitioning SDA from low to high while SCL is high. The bus is then free for communication with another SMBus or I²C device.

Acknowledge

The Acknowledge signal is used for handshaking between the master and the slave. An Acknowledge (active LOW) generated by the slave lets the master know that the latest byte of information was received. The corresponding SCL clock pulse is always generated by the master. The master releases the SDA line (HIGH) during the Acknowledge clock pulse. The slave must pull down the SDA line during the Acknowledge clock pulse so that it remains a stable LOW during the HIGH period of this clock pulse. When the master is reading from a slave device, it is the master's responsibility to acknowledge receipt of the data byte in the bit that follows unless the transaction is complete. In that case the master will decline to acknowledge and issue the STOP condition to terminate the communication.

Write Byte Protocol

The master initiates communication to the LTC4259 with a START condition and a 7-bit bus address followed by the Write Bit (Wr) = 0. If the LTC4259 recognizes its own address, it acknowledges and the master delivers the command byte, signifying to which internal LTC4259 register the master wishes to write. The LTC4259 acknowledges and latches the lower five bits of the command byte into its Register Address register. Only the lower five bits of the command byte are checked by the LTC4259; the upper three bits are ignored. The master then delivers the data byte. The LTC4259 acknowledges once more and latches the data into the appropriate control register. Finally, the master terminates the communication with a STOP condition. Upon reception of the STOP condition, the Register Address register is cleared (see Figure 7).

Read Byte Protocol

The master initiates communication from the LTC4259 with a START condition and the same 7-bit bus address followed by the Write Bit (Wr) = 0. If the LTC4259 recognizes its own address, it acknowledges and the master delivers the command byte, signifying which internal LTC4259 register it wishes to read from. The LTC4259 acknowledges and latches the lower five bits of the command byte into its Register Address register. At this time the master sends a REPEATED START condition and the same 7-bit bus address followed by the Read Bit (Rd) = 1. The LTC4259 acknowledges and sends the contents of the requested register. Finally, the master declines to acknowledge and terminates communication with a STOP condition. On the reception of the STOP condition, the Register Address register is cleared (see Figure 8).

Receive Byte Protocol

Since the LTC4259 clears the Register Address register on each STOP condition, the interrupt register (register 0) may be read with the Receive Byte Protocol as well as with the Read Byte Protocol. In this protocol, the master initiates communication with the LTC4259 with a START condition and a 7-bit bus address followed by the Read Bit (Rd) = 1. The LTC4259 acknowledges and sends the contents of the interrupt register. The master then declines to acknowledge and terminates communication with a STOP condition (see Figure 9).

Alert Response Address and the INT Pin

In a system where several LTC4259s share a common INT line, the master can use the Alert Response Address (ARA) to determine which LTC4259 initiated the interrupt.

The master initiates the ARA procedure with a START condition and the 7-bit ARA bus address (0001100)b followed by the Read Bit (Rd) = 1. If an LTC4259 is

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asserting the $\overline{\text{INT}}$ pin, it acknowledges and sends its 7-bit bus address $(010A_3A_2A_1A_0)$b and a 1 (see Figure 10). While it is sending its address, it monitors the SDAIN pin to see if another device is sending an address at the same time using standard I^2C bus arbitration. If the LTC4259 is sending a 1 and reads a 0 on the SDAIN pin on the rising edge of SCL, it assumes another device with a lower address is sending and the LTC4259 immediately aborts its transfer and waits for the next ARA cycle to try again. If transfer is successfully completed, the LTC4259 will stop pulling down the $\overline{\text{INT}}$ pin. When the $\overline{\text{INT}}$ pin is released in this way or if a 1 is written into the Clear Interrupt pin bit (bit 6 of register 1Ah), the condition causing the LTC4259 to pull the $\overline{\text{INT}}$ pin down must be removed before the LTC4259 will be able to pull $\overline{\text{INT}}$ down again. This can be done by reading and clearing the event registers or by writing a 1 into the Clear All Interrupts bit (bit 7 of register 1Ah). The state of the $\overline{\text{INT}}$ pin can only change between I^2C transactions, so an interrupt is cleared or new interrupts are generated after a transaction completes and before new I^2C bus communication commences. Periodic polling of the alert response address can be used instead of the $\overline{\text{INT}}$ pin if desired. If any device acknowledges the alert response address, then the $\overline{\text{INT}}$ line, if connected, would have been low.

System Software Strategy

Control of the LTC4259 hinges on one decision, the LTC4259's operating mode. The three choices are described under Operating Modes. In Auto mode the LTC4259 can operate autonomously without direction from a host controller. Because LTC4259s running in Auto mode will power every valid PD connected to them, the PSE must have 15.4W/port available. To reduce the power requirements of the –48V supply, PSE systems can track power usage, only turning on ports when sufficient power is available. The IEEE describes this as a power allocation algorithm and places two limitations: the PSE shall not power a PD unless it can supply the maximum power for that PD's class and power allocation may not be based

solely on a history of each PD's power consumption. In order for a PSE to implement power allocation, the PSE's processor/controller must control whether ports are powered—the LTC4259's cannot operate in Auto mode. Semiauto mode fits the bill as the LTC4259 automatically detects and classifies PDs and makes this information available to the host controller, which decides to apply power or not. Operating the LTC4259 in Manual mode also lets the controller decide whether to power the ports but the controller must also control detection and classification. If the host controller operates near the limit of its computing resources, it may not be able to guide a Manual mode LTC4259 through detect, class and port turn-on in less than the IEEE maximum of 950ms.

In a typical PSE, the LTC4259s will operate in Semiauto mode as this allows the host to decide to power a port without burdening the controller. With an interrupt mask of F4h, the LTC4259 will signal to the host after it has successfully detected and classed a PD, at which point the host can decide whether enough power is available and command the LTC4259 to turn that port on. Similarly, the LTC4259 will generate interrupts when a port's power is turned off. By reading the LTC4259's interrupt register, the host can determine if a port was turned off due to overcurrent (t_{START} or t_{ICUT} faults) or because the PD was removed (Disconnect event). The host then updates the amount of available power to reflect the power no longer consumed by the disconnected PD. Setting the MSB of the interrupt mask causes the LTC4259 to communicate fault conditions caused by failures within the PSE, so the host does not need to poll to check that the LTC4259s are operating properly. This interrupt driven system architecture provides the controller with the final say on powering ports at the same time, minimizing the controller's computation requirements because interrupts are only generated when a PD is discovered or on a fault condition.

The LTC4259 can also be used to power older powered Ethernet devices that are not 802.3af compliant and may be detected with other methods. Although the LTC4259

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does not implement these older detection methods automatically, if software or external circuitry can detect the noncompliant devices, the host controller may command the LTC4259 to power the port, bypassing IEEE compliant detection and classification and sending power to the noncompliant device.

LOGIC LEVEL SUPPLY

Aside from the 48V used to source power down Ethernet cables connected to each port, a logic level supply is required to power the digital portion of the LTC4259. To simplify design and meet voltage isolation requirements, the logic level supply can be generated from the isolated –48V supply. Figure 19 shows an example method using an LT®1619 to control a –48V to 3.3V current mode supply. This boost converter topology uses the LT1619 current mode controller and a current mirror which reflects the 3.3V output voltage to the –48V rail, improving the regulation tolerance over the more traditional large resistor voltage divider. This approach achieves

high accuracy with a transformerless design yielding high performance (tight regulation).

IEEE 802.3af COMPLIANCE

The LTC4259 is designed to control power delivery in IEEE 802.3af compliant Power Sourcing Equipment (PSE). Because proper operation of the LTC4259 may depend on external signals and power sources, like the –48V supply (V_{EE}) or the OSCIN oscillator source, external components such as the sense resistors (R_S), and possibly software running on an external microprocessor, using the LTC4259 in a PSE does not guarantee 802.3af compliance. Using an LTC4259 does get you most of the way there. This section discusses the rest of the elements that go along with the LTC4259 to make an 802.3af complaint PSE. Each paragraph below addresses a component which is critical for PSE compliance as well as possible pitfalls that can cause a PSE to be noncompliant. For further assistance please contact Linear Technology's Applications department.
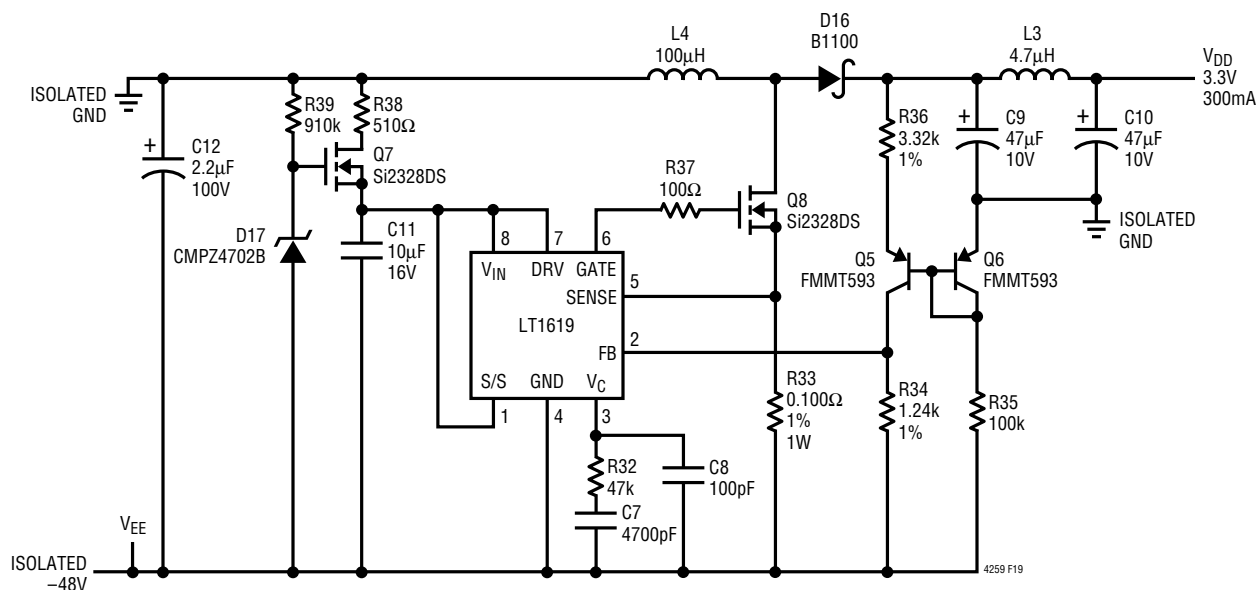

Figure 19. –48V to 3.3V Boost Converter

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Sense Resistors

The 0.5Ω resistors (R_S) used to sense the current through a port affect the current limit and all thresholds for a powered port. An error in the value of a sense resistor can cause noncompliance to the IEEE specifications for I_{INRUSH}/I_{LIM}, I_{CUT} and I_{MIN}. The value of the R_S resistor has been kept small to minimize power loss, allowing low cost resistors to be used. As a consequence, the SENSE voltages which the LTC4259 must measure are small. At the same time up to 450mA may be flowing through the sense resistors and associated circuit board traces. To prevent parasitic resistance of the circuit board's traces from obscuring the voltage drop across the sense resistor, the LTC4259 must Kelvin sense the sense resistor voltage. One way to achieve Kelvin sensing is "star grounding," shown pictorially in Figure 1. Another option is to connect the sense resistor and the LTC4259's V_{EE} pin to a −48V power plane in the circuit board. Either or these strategies will prevent voltages developed across parasitic circuit board resistances from affecting the LTC4259's current sense.

Power MOSFETs

The LTC4259 controls power MOSFETs in order to regulate current flow through the Ethernet ports. Under certain conditions these MOSFETs have to dissipate significant power. See the Choosing External MOSFETs section for a detailed discussion of the requirements these devices must meet.

Common Mode Chokes

Both nonpowered and powered Ethernet connections achieve best performance (for data transfer, power transfer and EMI) when a common mode choke is used on each port. In the name of cost reduction, some designs share a common mode choke between two adjacent ports. Even for nonpowered Ethernet, sharing a choke is not recommended. Now that two ports pass through the choke, it cannot limit the common mode current of either port. Rather the choke only controls the sum of both ports common mode current. Because cabling from the ports generally connects to different devices up to 200m apart, a current loop can form. In such a loop, common mode current flows in one port and out the other, and choke will not stop it because the sum of the currents is zero. Another way to view this interaction between the paired ports is that the choke acts as a transformer coupling the ports common modes together. In nonpowered Ethernet common mode current results from nonidealities like ground loops; it is not part of normal operation. However Power over Ethernet sends power and hence significant current through the ports; common mode current is a byproduct of normal operation. As described in the Choosing External MOSFETs section and under the Power Supplies heading below, large transients can occur when a port's power is turned on or off. When a powered port is shorted (see Surge Suppressors and Circuit Protection), a port's common mode current may be excessive. Sharing a common mode choke between two ports couples start-up, disconnect and fault transients from one port to the other. The end result can range from momentary noncompliance with 802.3af to intermittent behavior and even to excessive voltages that may damage circuitry (in both the PSE and PD) connected to the ports.

Detect, AC Blocking and Transient Supressor Diodes

During detection and classification, the LTC4259 senses the port voltage through the detect diodes, D_{DET} in Figure 16. Excessive voltage drop across D_{DET} will corrupt the LTC4259's detect and classification results. Select a diode for D_{DET} that will have less than 0.7V of forward drop at 0.4mA and less than 1V of forward drop at 50mA.

The AC blocking diodes can interfere with AC disconnect sensing if they become leaky. If the AC blocking diode, D_{AC} in Figure 16, begins leaking, it contributes to the Ethernet port impedance, potentially bringing the impedance low enough to draw I_{ACDMIN} from the DETECT pin and keep the port powered. More likely, leakage through the AC blocking diode will cause shifts in the AC disconnect threshold that are not large enough to make the PSE noncompliant. Generally, diode leakage is caused by voltage or temperature stress. Diodes that are rated to 100V or more and can

APPLICATIONS INFORMATION

handle dissipating at least 0.5W should not be stressed in this application. Other component leakages can have a similar affect on AC disconnect and affect DC disconnect if the leakage becomes more severe. Among components to be wary of are the transient surge suppressors. The devices shown in Figure 1 are rated for less than 5µA of leakage at 58V. However there is a potential for stress induced leakage, so healthy margins should be used when selecting diodes for these applications.

Capacitors

Sizing of both the C_{DET} and C_{PSE} capacitors is critical to proper operation of the LTC4259's AC disconnect sensing. See the AC Disconnect section for more information. Also, C_{PSE} may be important to the voltage stability of a powered port. Port voltage instability is generally not a problem if V_{EE}, the –48V supply, is well bypassed. For both of these reasons be aware that many ceramic dielectrics have dramatic capacitance versus DC voltage coefficients. A 0.22µF ceramic capacitor is often nowhere near 0.22µF when operating at 50VDC or 100VDC. Use 100V or higher rated X7R capacitors for C_{DET} and C_{PSE} as these have reduced voltage dependance while also being small and inexpensive.

Power Supplies

The LTC4259 must be supplied with 3.3V (V_{DD}) and –48V (V_{EE}). Poor regulation on either of these supplies can lead to noncompliance. The IEEE requires a PSE output voltage between 44V and 57V. Allowing for voltage drop, mostly across the AC blocking diodes D_{AC} between V_{EE} and the PSE's Ethernet jacks, means that V_{EE} must be more negative than –45V (more if D_{AC} has more than 1V of forward drop). When the LTC4259 begins powering an Ethernet port, it controls the current through the port to minimize disturbances on V_{EE}. However if the V_{EE} supply is underdamped or otherwise unstable, its voltage could go outside of the IEEE specified limits causing all ports in the PSE to be noncompliant. This scenario can be even worse when a PD is unplugged because the current drops immediately to zero. In both cases the V_{EE} supply must

always stay between –45V and –57V. In addition, the 802.3af specification places specific ripple, noise and load regulation requirements on the PSE. Among other things, disturbances on either V_{DD} or V_{EE} can adversely affect detection, classification and the AC disconnection sensing. In short, proper bypassing and stability of the V_{DD} and V_{EE} supplies are important.

Another problem that can affect the V_{EE} supply is insufficient power, leading to the supply voltage drooping out of the specified range. The 802.3af specification states that if a PSE powers a PD it must be able to provide the maximum power level requested by the PD based on the PD's classification. The specification does allow a PSE to choose not to power a port because the PD requires more power than the PSE has left to deliver. If a PSE is built with a V_{EE} supply capable of less than 15.4W • (number of PSE's Ethernet ports), it must implement a power allocation algorithm that prevents ports from being powered when there is insufficient power. Because the specification also requires the PSE to supply 400mA at up to a 5% duty cycle, the V_{EE} supply capability should be at least a few percent more than the maximum total power the PSE will supply to PDs. Finally, the LTC4259's draw current from V_{EE}. If the V_{DD} supply is generated from V_{EE}, that power divided by the switcher efficiency must be added to the V_{EE} supply's capability; (33mW ÷ efficiency • [number of PSE's Ethernet ports] ÷ 4) typically less than 12mW/port.

AC disconnect also relies on an oscillating signal applied to the OSCIN pin. Requirements for this signal are provided in the OSCIN Input and Oscillator Requirements section. Out-of-band noise on the OSCIN pin will disrupt the LTC4259's ability to sense the absence of a PD. Any noise present at the OSCIN pin is amplified by the LTC4259 and driven out of the DETECT pins (of powered ports with AC disconnect enabled). Due to the amount of capacitance connected to the DETECT pins, driving this noise can easily require more than I_{ACDMIN}, tripping the DETECT pin current sense and keeping the port powered. During circuit board layout, keep wiring from the oscillator to the OSCIN pin away from noise sources like digital clock and

APPLICATIONS INFORMATION

data lines. Also a single-stage RC lowpass filter (shown in Figure 20) will attenuate out-of-band noise. There won't be much voltage drop across the RC filter because the impedance of the OSCIN pin is high, typically 500k.
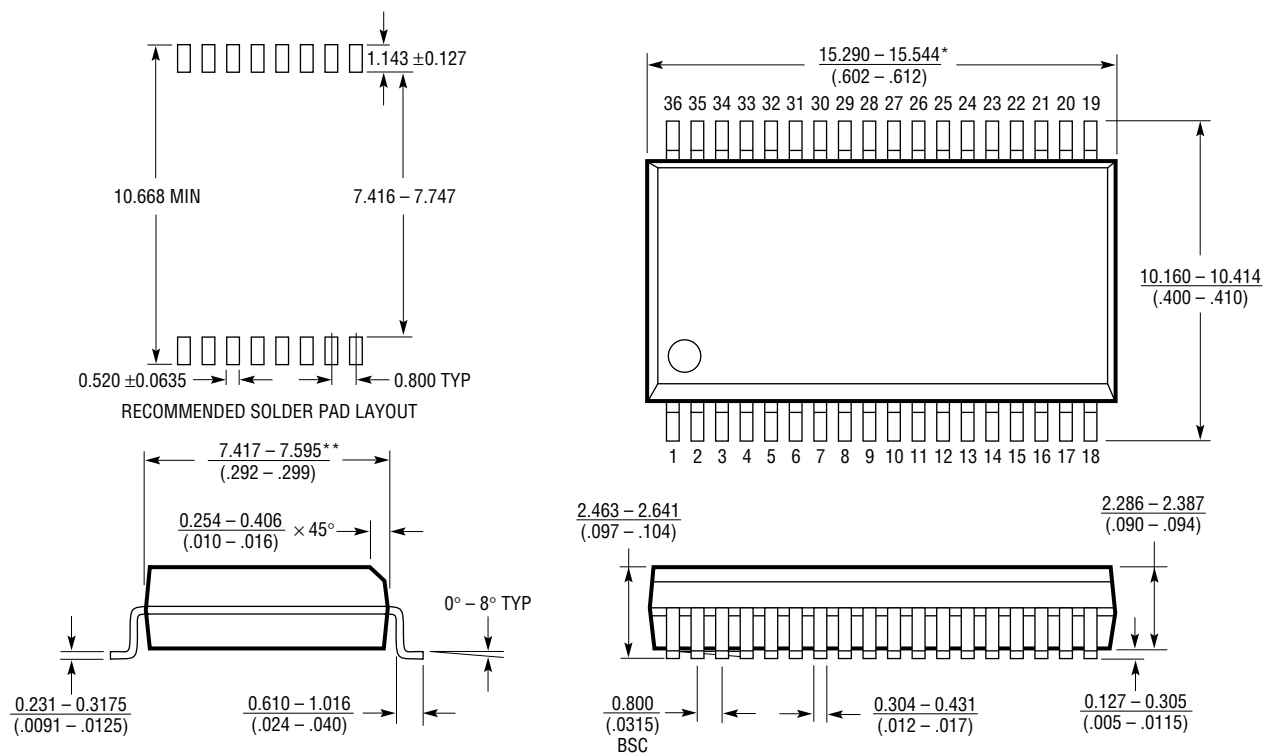
CONCLUSION

The LTC4259 provides the precision analog circuitry and logic necessary to build IEEE 803.3af compliant Power over Ethernet power sourcing equipment (PSE). The requirements placed on the PSE are complex and the LTC4259 handles most of them but there are elements of the PSE that are beyond the LTC4259's control.

These potential compliance pitfalls can be avoided during circuit design and layout by paying attention to the issues mentioned above. In addition, consider checking for IEEE 802.3af compliance after subjecting the PSE to real-world fault conditions: ESD and cable discharge events, shorted ports, connecting to an already powered port, power supply glitches and so on. Linear Technology's Applications department can also provide additional support.

LINEAR
TECHNOLOGY

PACKAGE DESCRIPTION

GW Package
36-Lead Plastic SSOP (Wide .300 Inch)
(Reference LTC DWG # 05-08-1642)

1.143 ±0.127

10.668 MIN

7.416 – 7.747

0.520 ±0.0635

0.800 TYP

RECOMMENDED SOLDER PAD LAYOUT

15.290 – 15.544*
(.602 – .612)

36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

10.160 – 10.414
(.400 – .410)

7.417 – 7.595**
(.292 – .299)

0.254 – 0.406
(.010 – .016) × 45°

0° – 8° TYP

0.231 – 0.3175
(.0091 – .0125)

0.610 – 1.016
(.024 – .040)

2.463 – 2.641
(.097 – .104)

2.286 – 2.387
(.090 – .094)

0.800
(.0315)
BSC

0.304 – 0.431
(.012 – .017)

0.127 – 0.305
(.005 – .0115)

GW36 SSOP 0502

NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS

2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH
SHALL NOT EXCEED 0.152mm (0.006") PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD
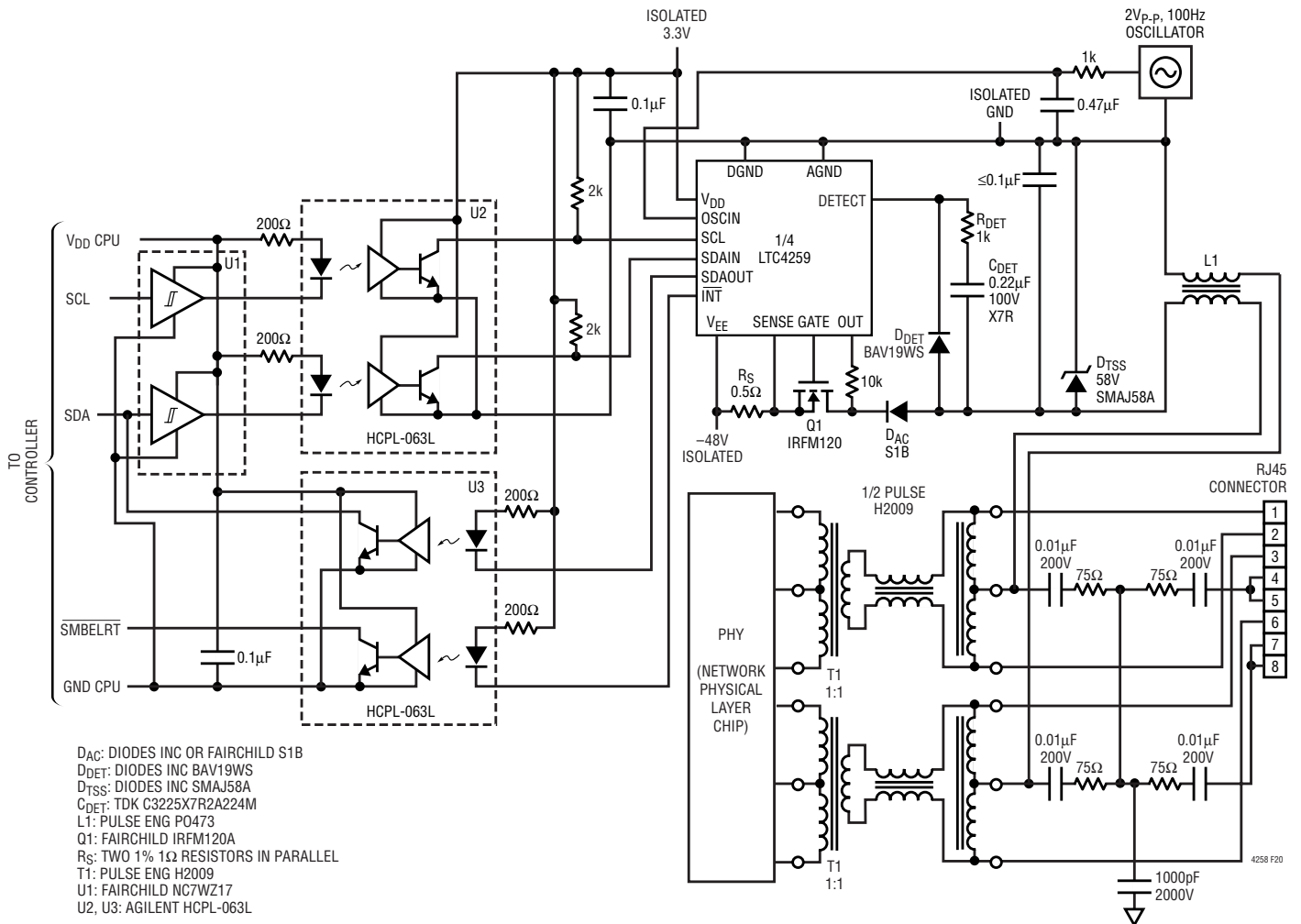FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

4259i

LINEAR
TECHNOLOGY

TYPICAL APPLICATION

DAC: DIODES INC OR FAIRCHILD S1B
DDET: DIODES INC BAV19WS
DTSS: DIODES INC SMAJ58A
CDET: TDK C3225X7R2A224M
L1: PULSE ENG PO473
Q1: FAIRCHILD IRFM120A
RS: TWO 1% 1Ω RESISTORS IN PARALLEL
T1: PULSE ENG H2009
U1: FAIRCHILD NC7WZ17
U2, U3: AGILENT HCPL-063L

Figure 20. One Complete Isolated Powered Ethernet Channel

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1619	Low Voltage Current Mode PWM Controller	
LTC1694	SMBus/I^{2}C Accelerator	
LTC4255	Quad Network Power Controller	Non-IEEE 802.3af Compliant Current Levels
LTC4257	IEEE 802.3af PD Interface Controller	Internal Switch, Programmable Classification
LTC4258	Quad Power Over Ethernet Controller	DC Disconnect Only

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com